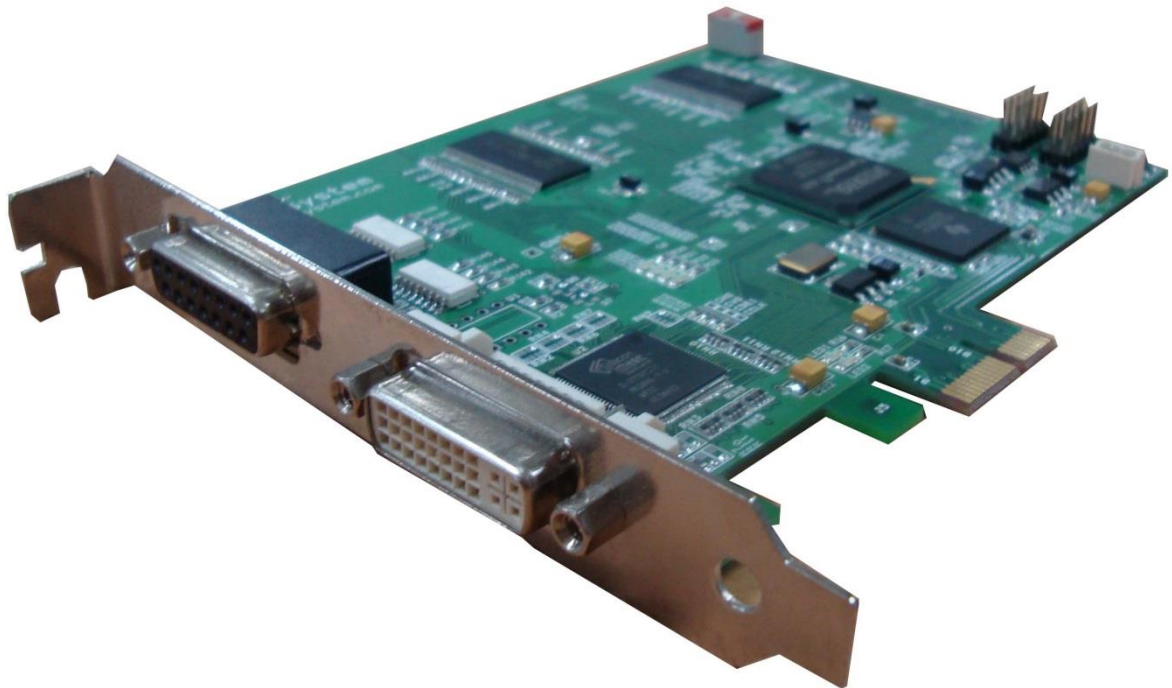


PCIe-FRM14

User Manual

Version 1.2



© 2005 DAQ SYSTEM Co., Ltd. All rights reserved.

Microsoft® is a registered trademark; Windows®, Windows NT®, Windows XP®, Windows 7®, Windows 8®, Windows 10®
All other trademarks or intellectual property mentioned herein belongs to their respective owners.

Information furnished by DAQ SYSTEM is believed to be accurate and reliable, However, no responsibility is assumed by DAQ SYSTEM for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or copyrights of DAQ SYSTEM.

The information in this document is subject to change without notice and no part of this document may be copied or reproduced without the prior written consent.

Contents

1. Introduction	-----	3
1-1 Product Features	-----	5
1-2 Product Application	-----	5
2. PCIe-FRM14 Board Function		
2-1 FPGA Block Diagram	-----	6
2-2 DVI(Digital Video Interface)	-----	7
3. PCIe-FRM14 Board Description		
3-1 Board Layout	-----	10
3-2 Device Features	-----	11
3-3 Connector Pin out	-----	12
3-3-1 CON1(DVI) Connector	-----	13
3-3-2 P1(D-Sub15) Connector	-----	15
3-3-3 SW1 Switch	-----	17
3-3-4 SW2 Switch	-----	17
3-3-5 J2 Connector	-----	17
3-3-6 J4 Connector	-----	17
3-4 Digital In/Out		
3-4-1 Photo-coupler Input	-----	18
3-4-2 Photo-coupler Output	-----	19
4. Installation		
4-1 Product Contents	-----	20
4-2 Installation Process	-----	21

5. Sample Program

5-1 Frm14Test Program	-----	25
5-1-1 Image Frame Function	-----	26
5-1-2 DIO Function	-----	26
5-2 Frm14View 프로그램	-----	27

Appendix

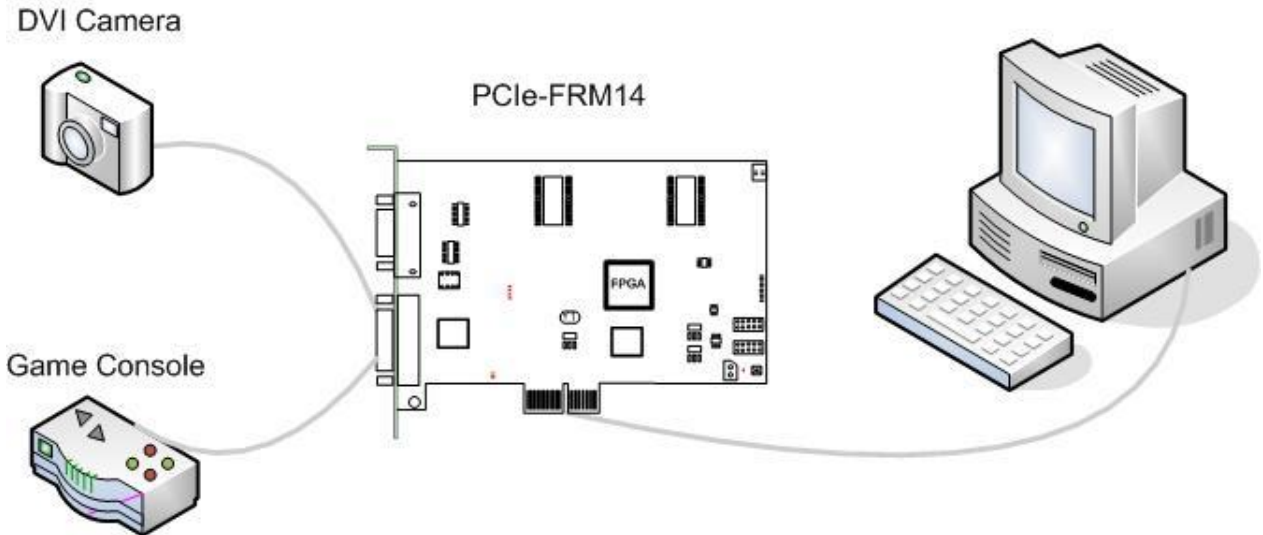
A-1 Board Size	-----	29
A-2 Repair Regulations	-----	30

References

-----	31
-------	----

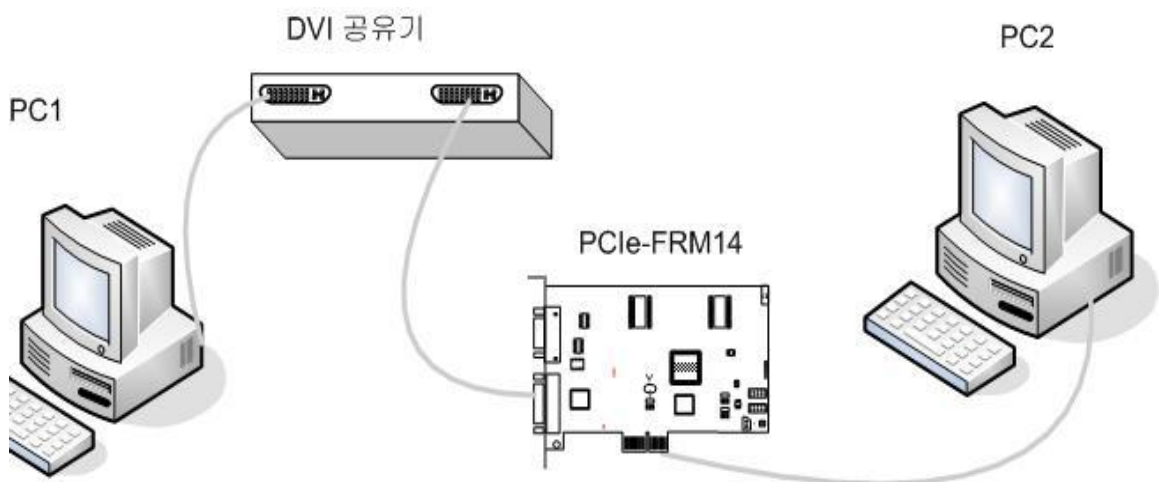
1. Introduction

PCIe-FRM14 is a Frame Grabber capture card with single link DVI/VGA input. This card is installed in a PCI Express slot and transfers captured data from video capture devices - DVI cameras, other LCD monitor inputs (using a splitter), game consoles, etc. - to the PC via the PCIe bus.



[Figure 1-1. PCIe-FRM14 Board Usage 1]

As shown in Figure [1-2], the PCIe-FRM14 is inserted into any available PCI Express slot in the PC2. The PCIe-FRM14 receives and outputs the data of the display of PC1 through PC2 application's program.



[Figure 1-2. PCIe-FRM14 Board Usage 2]

It receives DVI input from other devices and can check it on the PC. The operation of the board is controlled by the program API, and [Figure 1-3] shows the state when PCIe-FRM14 is interlocked with the actual device. It is interfaced with external I/O through the 15Pin D-SUB connector on the left, and is connected to the DVI connector at the bottom to send and receive frame data with the DVI transmitter.



[Figure 1-3. PCIe-FRM14 in Action]

1-1 Product Features

Items	Description	Remark
Hardware		
PC Interface	PCI Express 4x	
Operation Power	PC Power	+3.3V (Max 1.1A) +12V (Max 1A).
Video Interface	1 Port Single DVI	
Feature	Full HD 1080P at 12fps	MAX 1920x1200 resolution
External I/O	4-Ch Digital In 4-Ch Digital Out	Input : Voltage Range : 9 ~ 24V Current Range : 3.75mA (For 9V) ~ 10mA (For 24V) Digital Output : Voltage Range : ~ 7V Current Range : Within 10mA
On-board Memory	128MB DDR SDRAM	
Communication		
Simultaneous use of boards	Max. 4	
Software		
OS	Windows 2000/XP/7/8/10 (32/64bit)	
API	Windows Client DLL API	
Development		
Support	Sample Program	VC++
Environmental conditions		
Operating temperature range	0 ~ 60°C	
Storage temperature range	-20 ~ 80°C	
Humidity range	5 ~ 95%	Non-condensing
Board size	130mm X 106mm	PCB Board Size

1-2 Product Applications

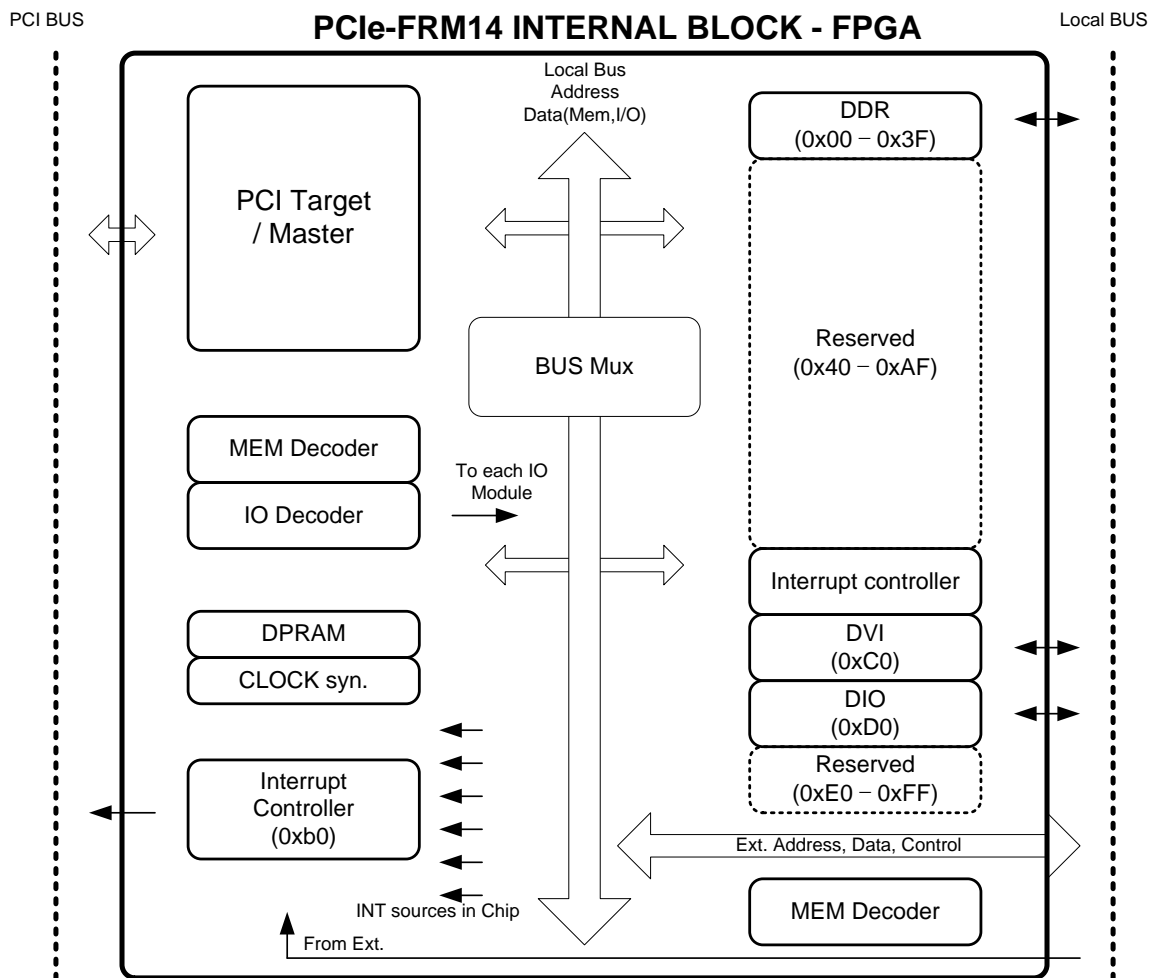
- Image recognition (Pattern, particle, etc.)
- Inspection equipment (Sensor, Semiconductor, Device etc.)
- Security Solution
- BLU-RAY
- Game Consoles

2. PCIe-FRM14 Board Function

2-1 FPGA Block Diagram

In the case of PCIe-FRM14, FPGA Core Logic is in charge of overall control. It receives RGB, HDMI (High-Definition Multimedia Interface), and DVI (Digital Visual Interface) signals as its main function and delivers it to the PC.

These functions are performed using API in PC through PCI Express 1x interface.



[Figure 2-1. PCIe-FRM14 Block Diagram]

The FPGA core logic is programmed using JTAG, and the logic program is saved in FPGA Program Logic and loaded when power is applied.

2-2 DVI (Digital Visual Interface)

DVI (Digital Visual Interface) is divided into DVI-D (Digital Only), DVI-A (Analog Only), and DVI-I (Integrated Digital & Analog) methods. The PCIe-FRM14 board supports DVI-I type DVI, so it is compatible with the existing analog type methods. Also, HDMI (High Definition Multimedia Interface) that uses the same format of digital image data can be used together by using the DVI to HDMI gender. [Figure 2-2. Reference]

However, some HDMI monitors may not display images output from devices that do not comply with the encryption standard for copyright protection called HDCP (High-bandwidth Digital Control Protection) high-bandwidth digital content protection.

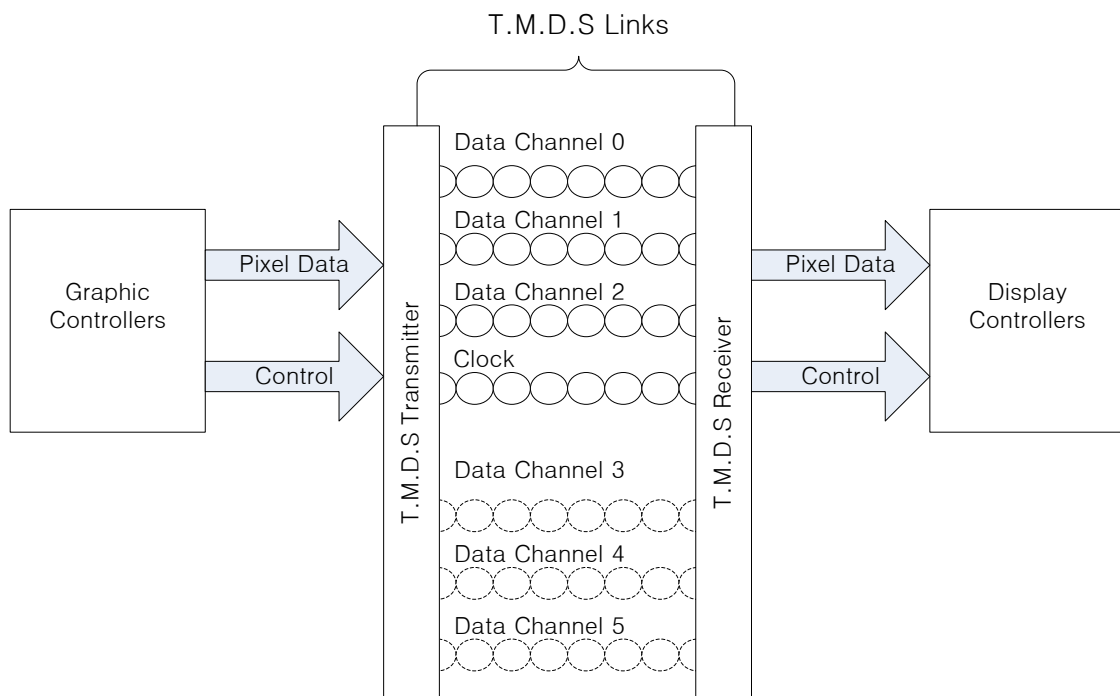


[Figure 2-2. DVI to RGB & DVI to HDMI Gender]

The data format of DVI is based on the Panel Link serial signal line. DVI uses a digital transmission protocol that is Transition Minimized Differential Signaling (TMDS) as shown in [Figure 2-2]. TMDS is composed of TMDS Transmitter and TMDS Receiver, and a Transmitter is mounted on the graphic card side and a Receiver is mounted on the monitor side to transmit digital data from the graphic card to the monitor.

DVI is divided into single DVI using Digital Channel 0 ~ 2 and Clock line, and Dual DVI using both signal lines of Digital Channel 3 ~ 5. For single DVI, it supports up to WUXGA (1920 x 1200 @60Hz) and has a bandwidth of 3.7Gbits/s. Dual DVI supports up to WQXGA (2560 x 1600 @60Hz) and has a bandwidth of 7.4Gbits/s. The advantage of DVI is that it can transmit longer distances than LVDS (Low Voltage Differential Signaling) and can transmit a higher band signal.

A single DVI link has a maximum resolution of 2.6M pixels at 60Hz. The single link maximum is fixed at 165 MHz, so all displays slower than this use single link mode, and faster than this will switch to dual link mode.



[Figure 2-3. T.M.D.S Logical Links]

PCle-FRM14 supports single DVI. PCIe-FRM14 board supports DVI-I type DVI, so it is compatible with existing analog type methods. can [Refer to Section 3.3 Connector Pin out for DVI connector and signal line]

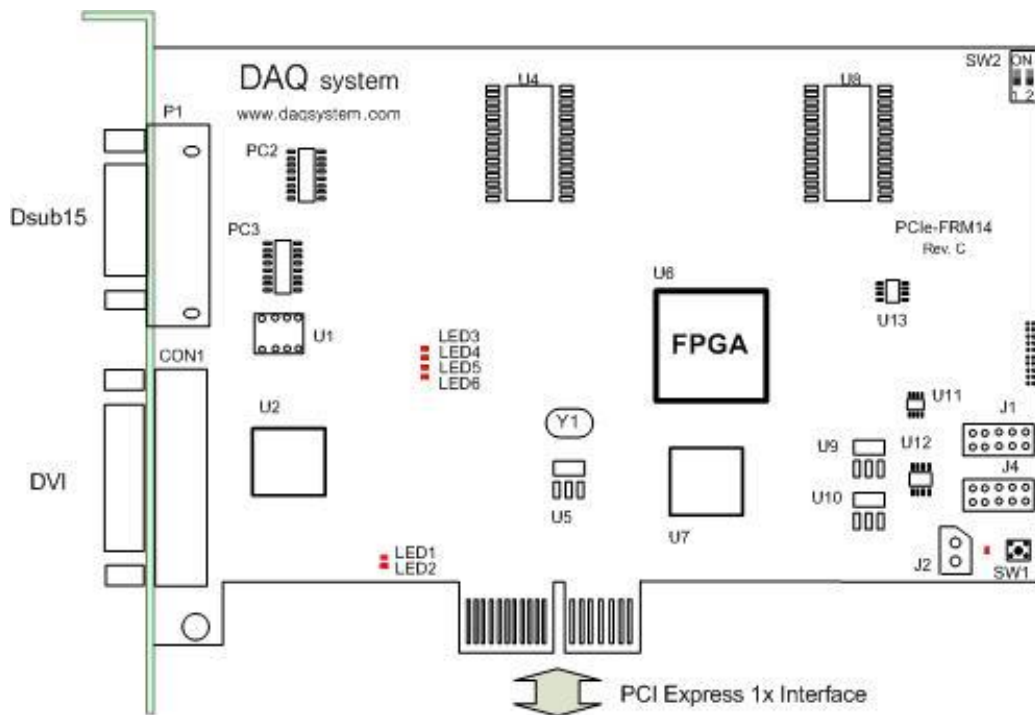
Control signal line consists of LVAL (Line Valid), FVAL (Frame Valid), DVAL (Data Valid) and clock, and transmits the valid horizontal and vertical resolution and data of the image to be transmitted according to the clock.

TMDS Receiver such as monitor and TMDS Transmitter such as graphic card have EDID (Extended Display Identification Data) standard for data communication between the output of the source device and the display. That is, display information is transferred from a display side such as a monitor to a host such as a frame grabber. EDID of the display is defined as a 128-byte (256-byte for EDID 2.0) data structure that contains information such as the relevant manufacturer and product identification block, display medium, color characteristics, and stable timing. EDID transmission method generally uses I2C.

3. PCIe-FRM14 Board Description

Each important board function is briefly described. For detailed function information, please refer to the parts specification.

3-1 PCIe-FRM14 Board Layout



[Figure 3-1. PCIe-FRM14 Layout]

There are a total of six LEDs on the board, the most important of which is LED5, and the description of each is as follows.

LED1 : Lights up when wake-up the board.

LED2 : Lights up when the board is reset.

LED3 : Lights up when frame data is being transmitted.

LED4 : Lights up when frame data is being transmitted.

LED5 : Lights up when the board finishes configuration and ready for operation.

3-2 Device Features

(1) **FPGA : U6**

All of the board functions are controlled by the Logic program of the FPGA.

(2) **DVI Receiver : U2**

Receives DVI Data and transmits it to FPGA.

(3) **Regulator : U5, U9, U10**

It supplies the power used by the board.

(4) **PCI Express Chipset : U7**

It is a bridge that processes PCI Express signals.

(5) **DDR Memory : U4, U8**

After saving DVI DATA in frame unit with a size of 128MByte, it is transmitted to PC through FPGA.

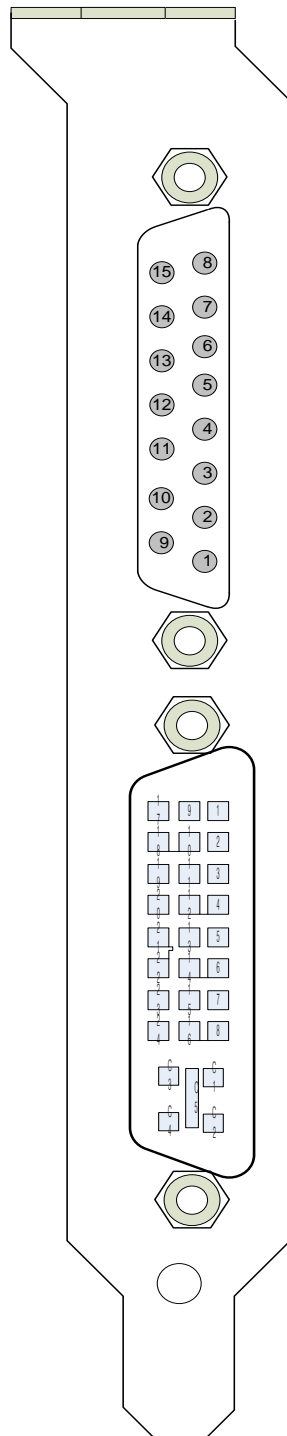
(6) **Photo-coupler Isolated I/O : PC2, PC3**

Configure an isolated input/output circuit for connection with an external device.

3-3 Connector Pin-out

The connectors and jumpers used in PCIe-FRM14 will be described. Main connectors include DVI connector CON1 for DVI connection and D-SUB 15pin connector for external I/O connection.

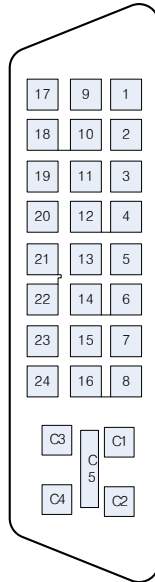
[Figure 3-2] shows the bracket that interfaces with the board and the connection connector.



[Figure 3-2. PCIe-FRM14 Front View]

3-3-1 CON1(DVI) Connector

[Figure 3-3] below shows the pin map of the DVI connector on the board. All pin specifications are input/output based on the DVI standard, so please refer to the DVI standard document for details.



[Figure 3-3. PCIe-FRM14 CON1 Connector Pin-out]

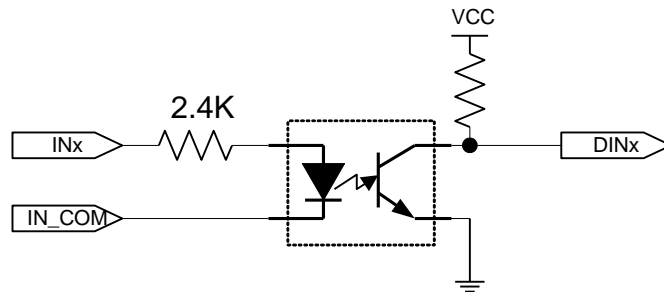
[Table 1. CON1 DVI Connector]

Pin #	Signal	Description
1	TMDS Data2-	Digital Red- (Link 1)
2	TMDS Data2+	Digital Red+ (Link 1)
3	TMDS Data2/4 Shield-	
4	TMDS Data4-	Digital Green- (Link 2)
5	TMDS Data4+	Digital Green+ (Link 2)
6	DDC Clock	Display Data Sync Clock
7	DDC Data	Display data channel (Display Information – Vendor/Product Identification EDID structure version Display media/features color, timing standard timing identification)
8	Analog V sync	Analog Vertical Sync
9	TMDS Data1-	Digital Green- (Link 1)
10	TMDS Data1+	Digital Green+ (Link 1)
11	TMDS Data1/3 Shield	

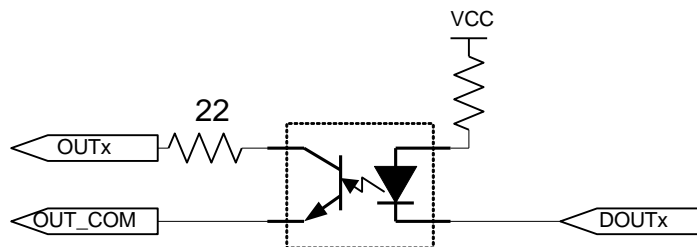
12	TMDS Data3-	Digital Blue- (Link 2)
13	TMDS Data3+	Digital Blue+ (Link 2)
14	+5V Power	Power for monitor standby
15	GND	Pin 14 and regression for synchronization
16	Hot Plug Detect	
17	TMDS Data0-	Digital Blue- (Link 1)
18	TMDS Data0+	Digital Blue+ (Link 1)
19	TMDS Data0/5 Shield	
20	TMDS Data5-	Digital Red- (Link 2)
21	TMDS Data5+	Digital Red+ (Link 2)
22	TMDS Clock Shield	
23	TMDS Clock+	Digital Clock+ (Link 1 & 2)
24	TMDS Clock-	Digital Clock- (Link 1 & 2)
C1	Analog Red	Analog Red (Disabled)
C2	Analog Green	Analog Green (Disabled)
C3	Analog Blue	Analog Blue (Disabled)
C4	Analog H sync	Analog Horizontal Sync (Disabled)
C5	Analog Ground	R, G, B signal regression (Disabled)

3-3-2 P1(D-Sub 15) Connector

On the PCIe-FRM14 board, 4 digital inputs and 4 digital outputs isolated by photo-couplers are available through the P1 connector. The circuit is as follows.



< Photo coupler input >



<Photo coupler output >

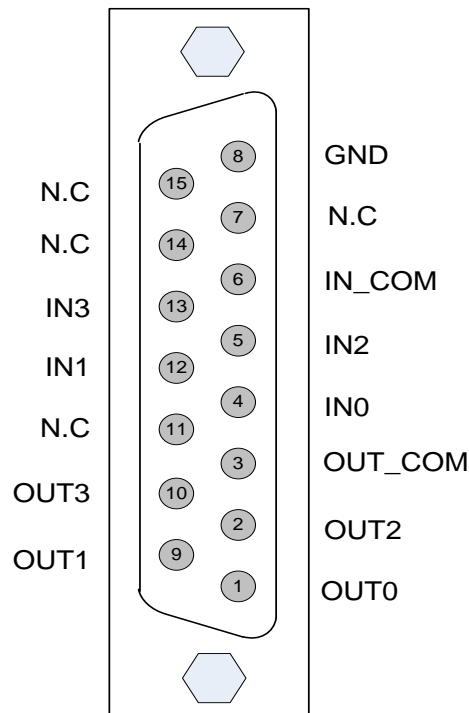
[Figure 3-4. Photo-coupler Input/Output Circuit]

For input, using a resistance of 2.4K ohm, about 5mA for 12V input and about 10mA for 24V input will flow. Available input voltage is within 9V to 24V.

The output uses a 22 ohm resistor to limit the maximum output current. Output current should be used within 10mA.

In special circumstances, the R value is adjusted and used to operate according to the above description.

The pin map of the connector is shown in the figure below.



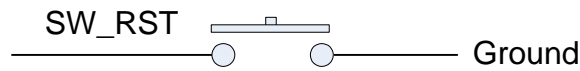
[Figure 3-5. D-SUB 15PIN pin-out]

[Table 2. D-Sub 15 Connector]

Pin No	Signal Name	Description	Remark
1	OUT0	Output 0	
2	OUT2	Output 2	
3	OUT_COM	Output Common	
4	IN0	Input 0	
5	IN2	Input 2	
6	IN_COM	Input Common	
7	N.C	No Connected	
8	GND	Ground	
9	OUT1	Output 1	
10	OUT3	Output 3	
11	N.C	No Connected	
12	IN1	Input 1	
13	IN3	Input 3	
14	N.C	No Connected	
15	N.C	No Connected	

3-3-3 SW1 Switch

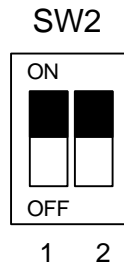
It is a Reset Switch that is Low Active.



[Figure 3-6. SW1 Switch]

3-3-4 SW2 Switch

The PCIe-FRM14 board is designed so that up to four PCIe-FRM14 boards can be used simultaneously in one system (PC). Each board classification can be set through the 4-pin DIP switch (SW2) in the board.



[Figure 3-7. SW2 Switch]

[Table 3. SW2 Description]

1	2	Description
OFF	OFF	Board No. 0
ON	OFF	Board No. 1
OFF	ON	Board No. 2
ON	ON	Board No. 3

3-3-5 J2 Connector (2Pin Header, 2.54mm)

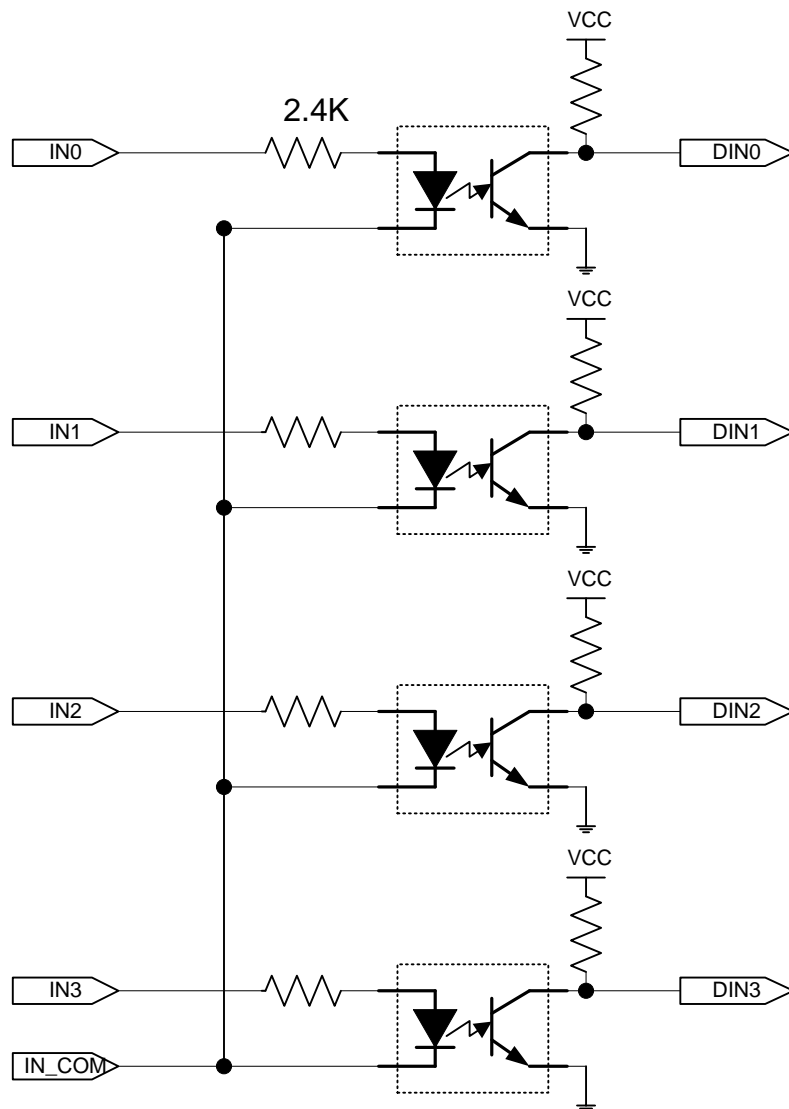
This is a 3.3V external DC power connector. This is the power used when installing the FPGA and is not normally used.

3.3.6 J4 Connector

J4 is a JTAG (Joint Test Action Group) connector and is used to update the FPGA program on the board. Do not use when operating the board normally.

3.4 Digital In/Out

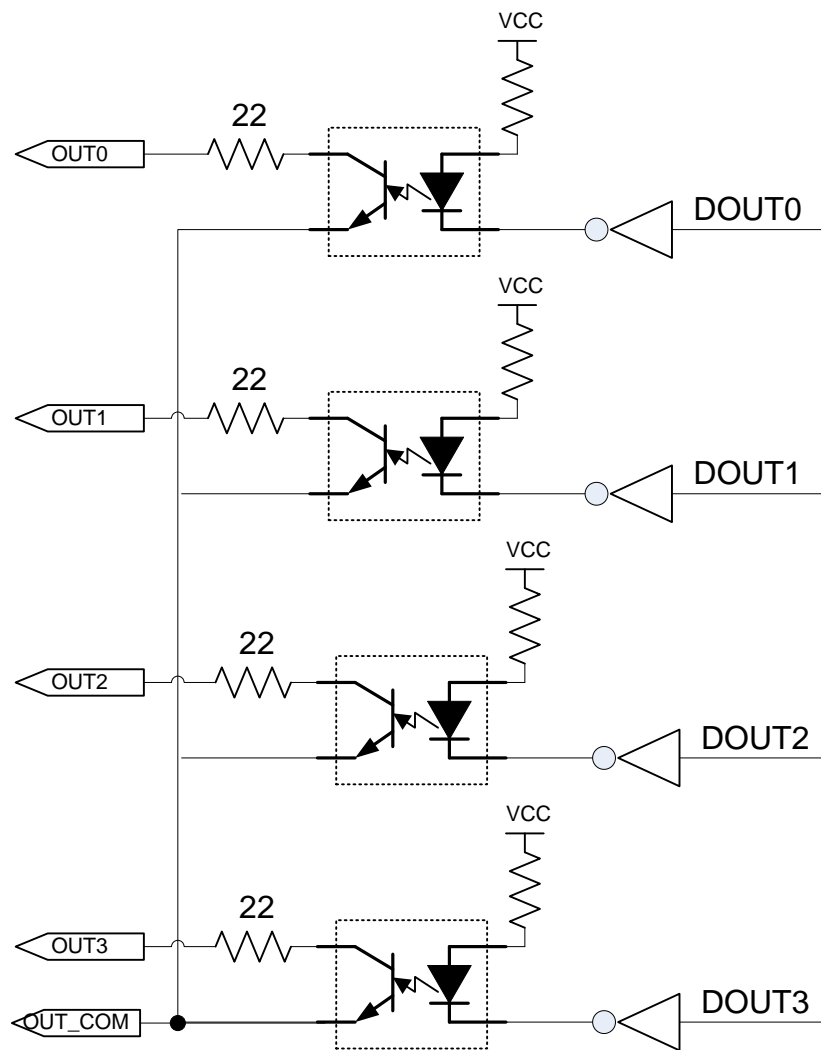
3-4-1 Photo-coupler Input



[Figure 3-8. Photo-coupler Digital Input circuit]

The photo-coupler input is input to the D-SUB 15-pin connector of the board, and in the program, DIO input bits 3 to 0 are connected as shown in the figure above.

3.4.2 Photo-coupler Output



[Figure 3-9. Photo-coupler Digital Output Circuit]

The photo-coupler output is output to the DSUB 15-pin connector of the board, and in the program, bits 3 to 0 of the DIO output are connected as shown in the figure above.

4. Installation

4-1 Product Contents

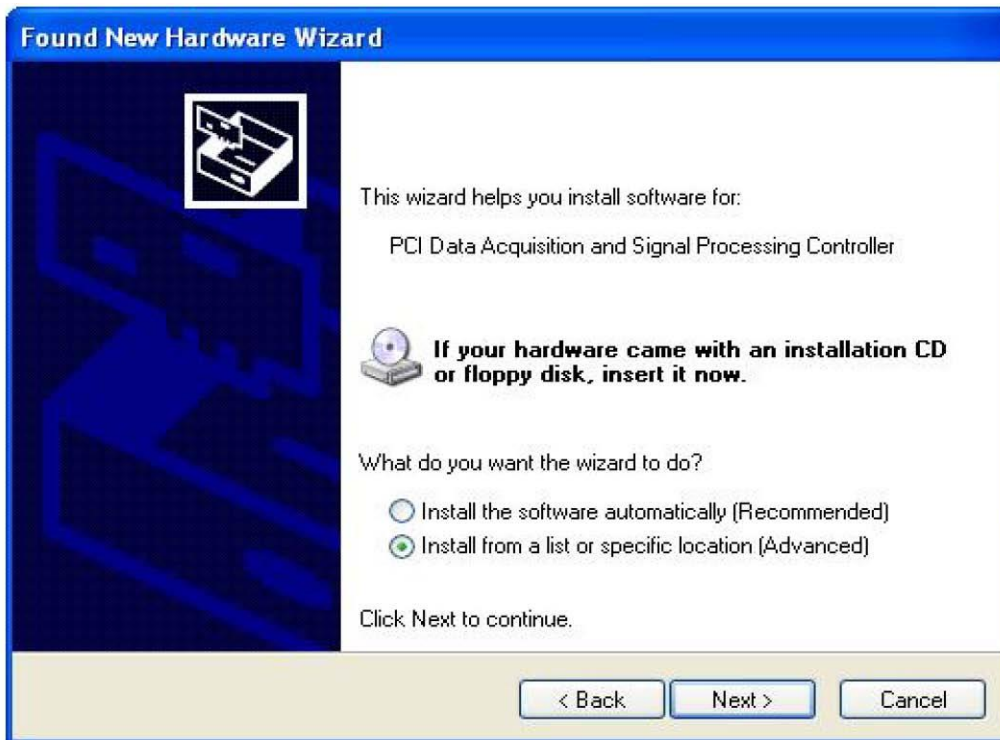
Before installing the board, check that the contents of the package are intact.

1. PCIe-FRM14 Board
 2. CD (Drivers/Manual/API/Sample source etc.)
 - Document Folder : Manual and Catalog
 - Driver Folder : pcie_frm14.sys pcie-frm14.inf
 - Readme Folder :
 - Sample Folder : Sample Application and DLL
 - TestApp Folder : Frm14Test.exe, Frm14View.exe
- ① Turn off the computer.
 - ② Remove the computer cover according to the computer manual.
 - ③ Insert the product into an empty PCI Express slot. If possible, insert the boards in the order closest to the CPU.
 - ④ After removing the blocked part at the back of the computer case in the slot where the board is inserted, tightly fasten the screws between the bracket of the board and the connection part of the case.
 - ⑤ In case of multi-board, repeat from step 3.

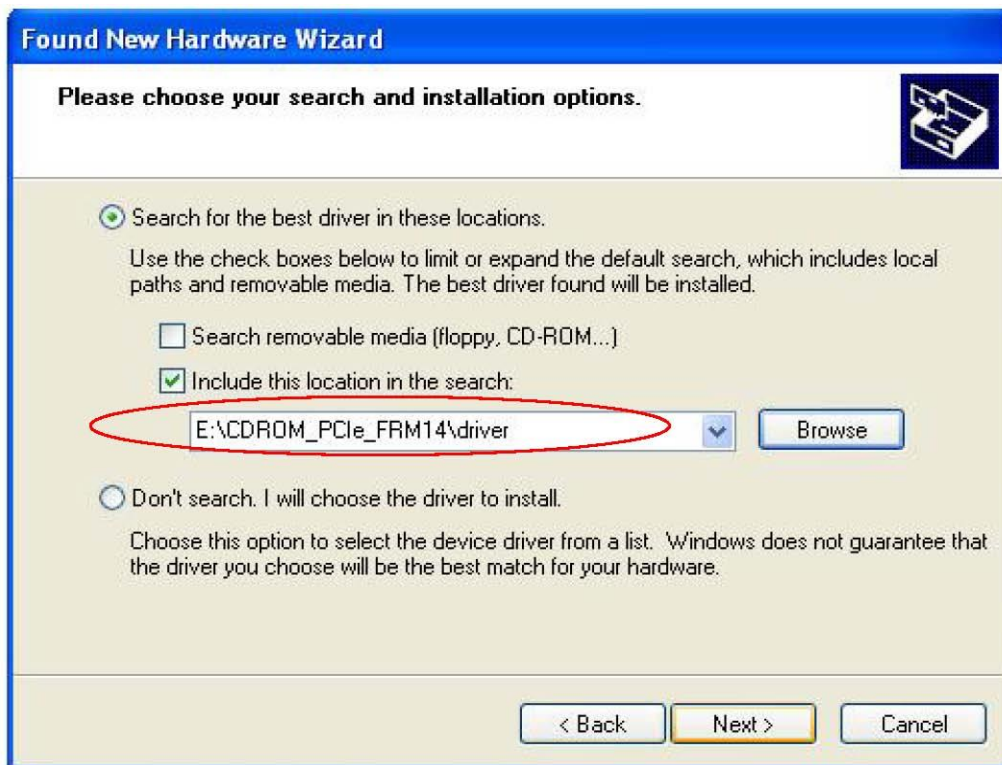
4-2 Installation Process

The board environment must be Windows 2000 SP4 or higher and Windows XP SP1 or higher. First, turn off the PC's power, plug the PCIe-FRM14 board into the PCI Express Slot, and turn on the PC's power. When the "Start New Hardware Wizard" window opens as shown below, select as shown below and click the Next button.

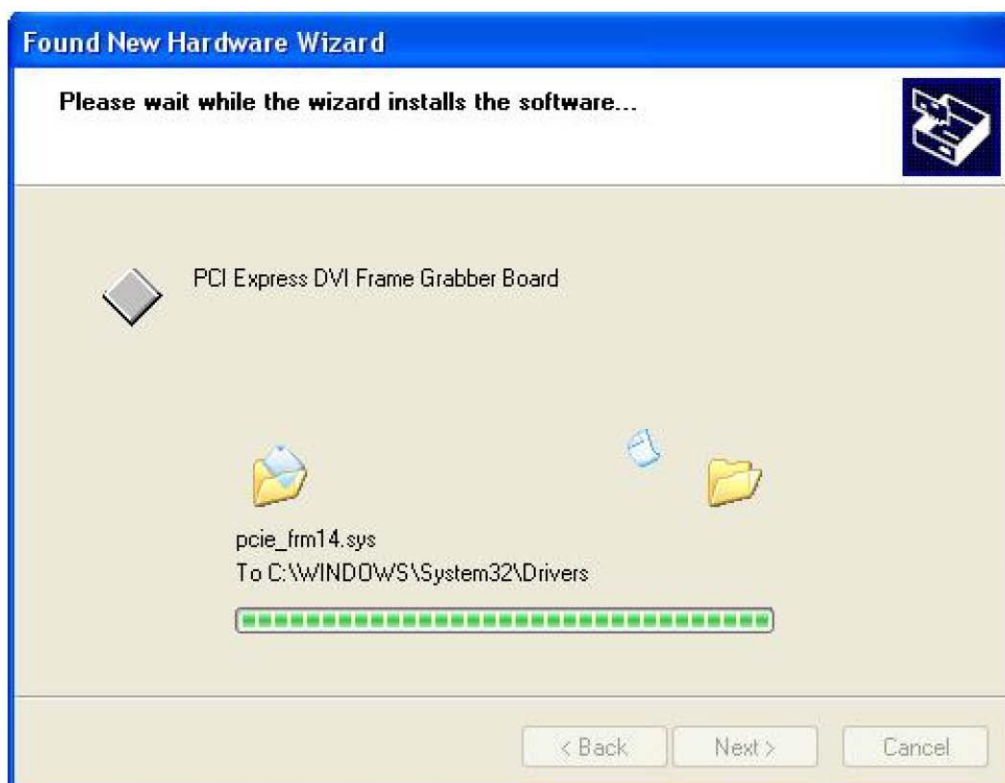
1. Select as below and click the Next button



2. Select Driver from the enclosed CD and click the Next button.



3. Click the Next button. It indicates that the installation process is proceeding as shown below. The driver folder contains "pcie_frm14.inf" and "pcie_frm14.sys" files required for driver installation. Click Next to install the driver files.

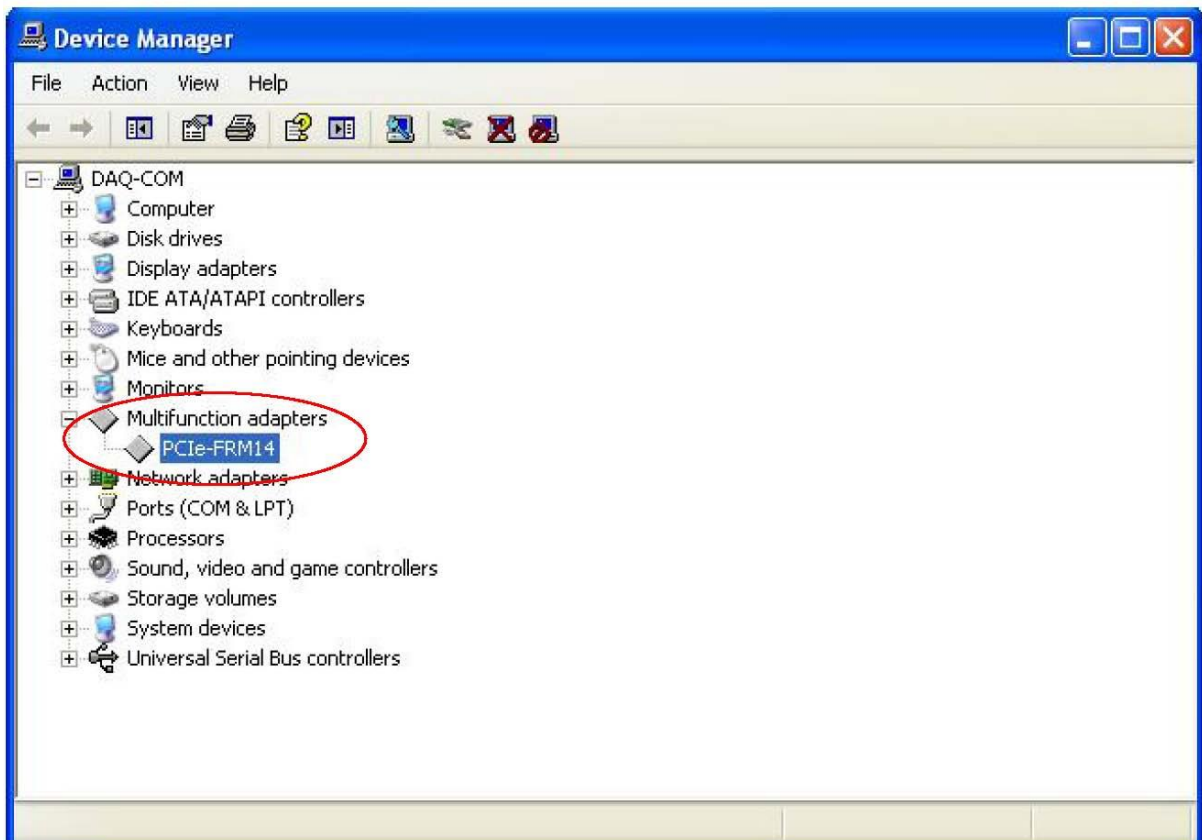


4. When the installation is completed normally, it is shown in the figure below.



5. When the installation is complete, check whether the driver is installed normally in the following way.
6. In My Computer -> Properties -> Hardware -> Device Manager, check if the **Multifunction Adapter** -> "PCIe-FRM14" is installed.

7. If it appears as shown in the figure below, the installation has been completed normally.



If you can see the "PCIe-FRM14" at Multifunction Adaptors, the driver installation is to have been over. (Check the red circle)

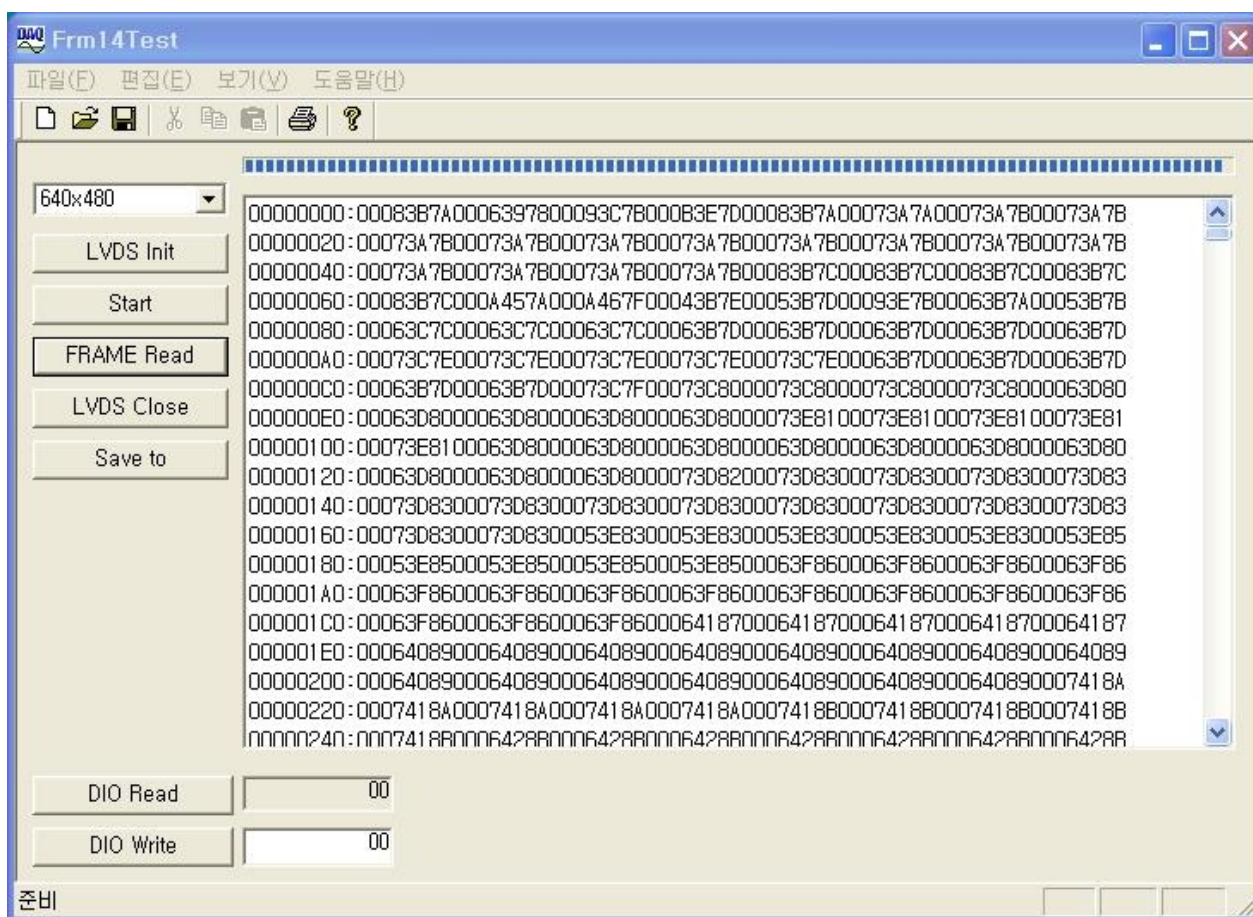
Notice : After installation, you should re-boot the system for the proper operation.

5. Sample Program

Sample programs **"Frm14Test.exe"** and **"Frm14View"** are provided in the TestApp folder of the CDROM provided with the board for easy use of the board. First, "Frm14Test.exe", one of the executable files, displays Frame Data as a hexadecimal value and stores it in memory or hard disk so that developers can utilize the frame data needed, and "Frm14View.exe" It is an executable file that shows the frame data as an image for the user to understand easily. In order to test the sample program, the driver of the board must be installed first.

The sample program is provided in the form of a source so that the API provided to use the board can be tested briefly, so the user can modify it and use it.

5-1 FrmTest Program



[Figure 5-1. Sample Program "Frm14Test.exe"]

API (Application Programming Interface) is required to use the above sample program. API is provided in the form of "DLL", and import library and header file are required for compilation.

All files specified above are included on the supplied CDROM. In order to run the sample program normally, the API DLL (PCIe-FRM14.DLL) must be in the folder of the executable file or in the Windows system folder or the folder specified by the Path environment variable.

5-1-1 Image Frame Function

(1) **'LVDS Init' button**

Press this button to initialize the function of receiving image frame data. It is performed only once after power is applied to the board.

(2) **'Start' button**

Press this button to begin to save image data.

(3) **'FRAME Read' button**

Press this button to read the image frame data of the board to your PC. If image frame data is not saved on the board, you must wait until the end of data collection.

(4) **'LVDS Close' button**

Press this button to finish usage of the board and terminate the program.

(5) **'Save to' button**

Press this button to save the image frame data of PC to a file.

5.1.2 DIO Function

(1) **'DIO Read' button**

Press this button to read the data on General Purpose I/O port. Reading Data are recorded the editor box beside the button

(2) **'DIO Write' button**

Press this button to write the data on General Purpose I/O port. You can directly write the data in the editor box beside the button.

5-2 Frm14View Program



[Figure 5-2. Sample Program "Frm14View.exe"]

API (Application Programming Interface) is required to use the above sample program. API is provided in the form of "DLL", and import library and header file are required for compilation.

All files specified above are included on the supplied CDROM. In order to run the sample program normally, the API DLL (PCI_FRM16.DLL) must be in the executable folder or in the Windows system folder or the folder specified by the Path environment variable.

[Figure 5-2] is a screen captured by connecting PCIe-FRM14 to the DVI connector of the graphic card of another system and executing "FrameView.exe" to capture the image displayed on the monitor.

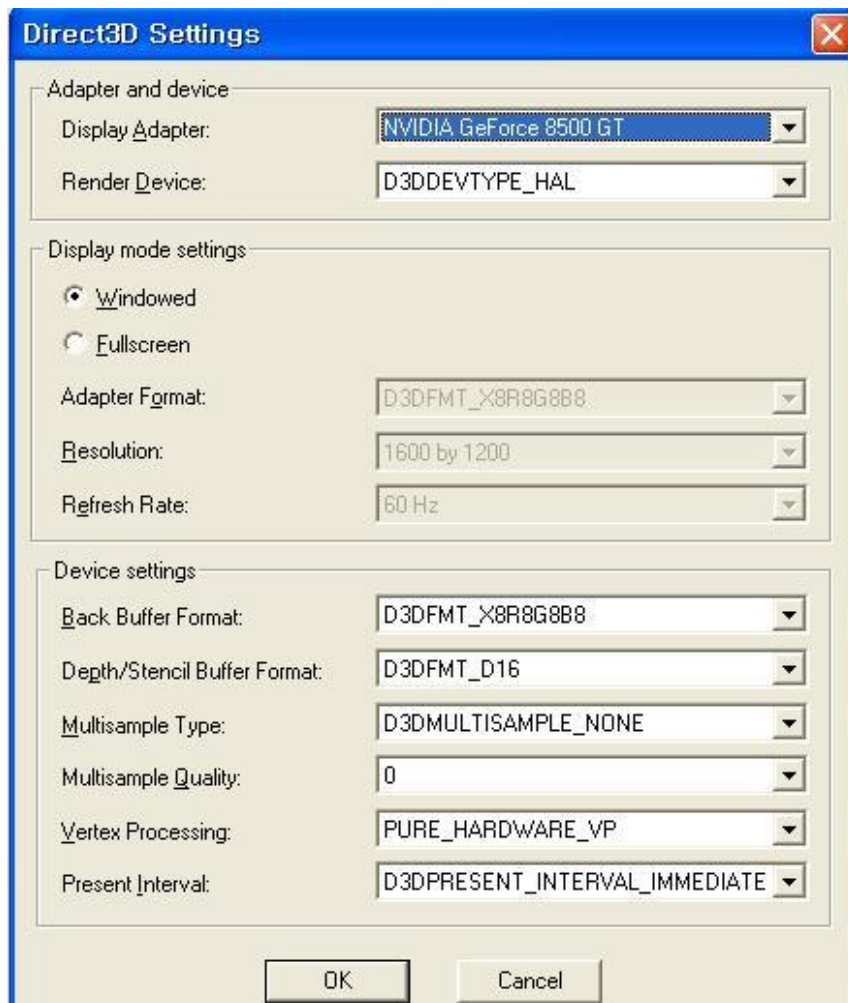
(1) Select resolution

Display resolution – Select it as fitted to input resolution.

Reverse --- Reverse On/Off

(2) Save --- Save to D:\frame.dat (It is fixed).

- (3) Stop --- Stop the saving.
- (4) Change Device --- Select a device which you wanted, if several devices are stick.



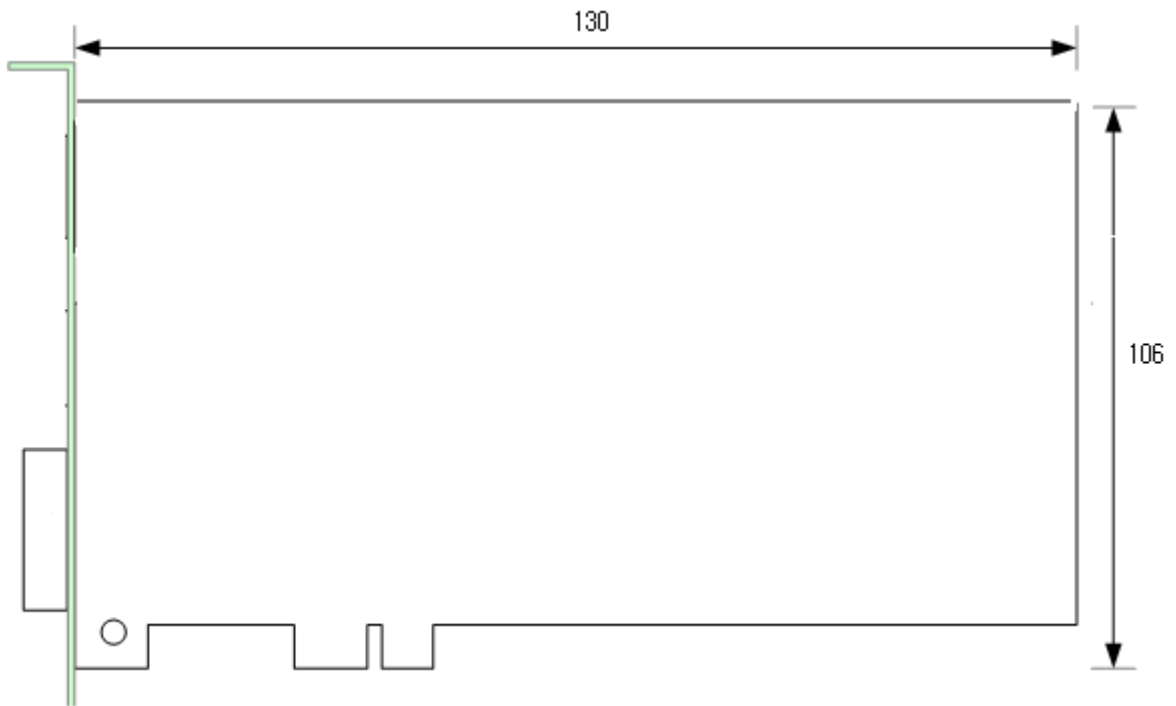
- (5) View Fullscreen --- A screen shows all over an image.
- (6) Board # selection --- Select a DVI Input number (0 : Bottom DVI, 1 : Upper DVI)
- (7) Device Start --- Start device which you selected.
- (8) Device Stop --- Stop device which you selected.
- (9) Exit --- Exit a program.

Appendix

A-1 Board Size

The external sizes of the board are as follows.

For detailed dimensions, please contact the person in charge.



A-2 Repair Regulations

Thank you for purchasing a DAQ SYSTEM product. Please refer to the following regarding Customer Service regulated by DAQ SYSTEM.

- (1) Read the user manual and follow the instructions before using the DAQ SYSTEM product.
- (2) When returning the product to be repaired, please write down the symptoms of the failure and send it to the head office.
- (3) All DAQ SYSTEM products have a 1-year warranty.
 - . Warranty period counts from the date the product is shipped from DAQ SYSTEM.
 - . Peripherals and third-party products not manufactured by DAQ SYSTEM are covered by the manufacturer's warranty.
 - . If you need repairs, please contact the Contact Point below..
- (4) Even during the warranty period, repairs are charged in the following cases..
 - ① Failure or damage caused by use without following the user's manual
 - ② Failure or damage caused by customer's negligence during product transportation after purchase
 - ③ Failure or damage caused by natural phenomena such as fire, earthquake, flood, lightning, pollution, or power supply exceeding the recommended range
 - ④ Failure or damage caused by inappropriate storage environment (e.g. high temperature, high humidity, volatile chemicals, etc.)
 - ⑤ Breakdown or damage due to unreasonable repair or modification
 - ⑥ Products whose serial number has been changed or removed intentionally
 - ⑦ If DAQ SYSTEM determines that it is the customer's fault for other reasons
- (5) Shipping costs for returning the repaired product to DAQ SYSTEM are the responsibility of the customer.
- (6) The manufacturer is not responsible for any problems caused by misuse, regardless of our warranty terms.

References

1. PCI Local Bus Specification Revision2.1
-- PCI Special Interest Group
2. How to install PCI DAQ Board
-- DAQ system
3. AN201 How to build application using API
-- DAQ system
4. AN312 PCIe-FRM14 API Programming
-- DAQ system

MEMO

Contact Point

Web sit : <https://www.daqsystem.com>

Email : postmaster@daqsystem.com

