PCI-FRM11

User Manual

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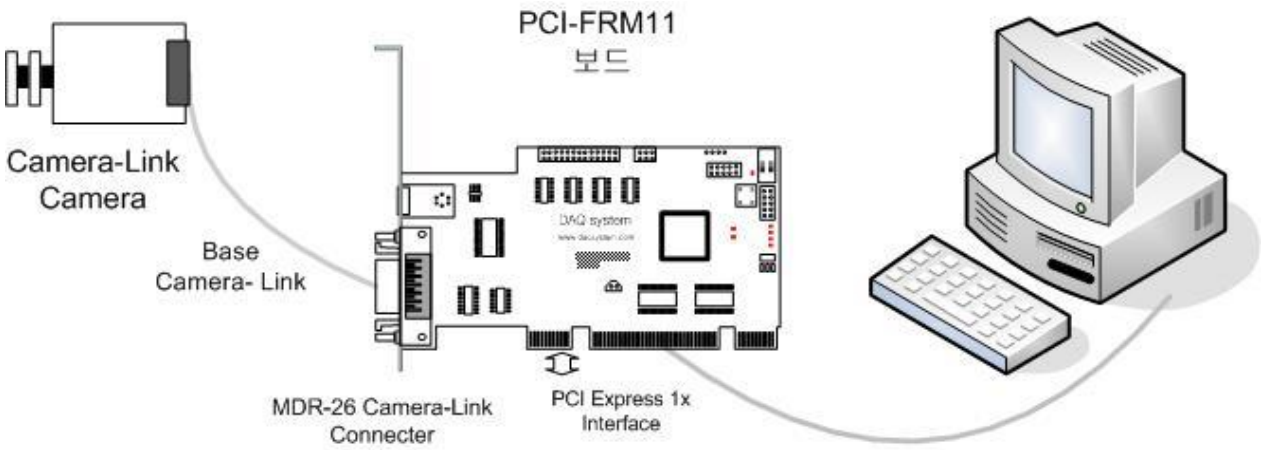
References

1. Introduction

PCI-FRM11 is a board that transmits the captured image frame to the PC through the PCI interface method in conjunction with the Camera-link standard camera.

The operation of the board is controlled by the program API, and the figure below shows the interlocking operation of the board.



[Figure 1-1. PCI-FRM11 Board Usage]

As shown in [Figure 1-1], PCI-FRM11 is installed in the PCI slot in the PC and receives from the camera through the image frame through the Camera-Link standard interface. It is responsible for transmitting the received data to the application program through the PCI interface.

1-1 Product Features

Items	Description	Remark
Hardware		
PC Interface	PCI Express 1x	
Operation Power	PC Power	+3.3V (Max 1.1A) +12V (Max 1A).
Video Interface	Base Camera Link	
Feature	Area Scan Camera Pixel Clock : 20 ~ 85MHz	
External I/O	4-Ch. Digital In 8-Ch Digital Out	Digital Input : Voltage Range : 9 ~ 24V Current Range : 3.75mA (For 9V) ~ 10mA (For 24V) Digital Output : Voltage Range : ~ 7V Current Range : Within 10mA
On-board Memory		
Communication	UART(Data bit 8, 1 start, 1 stop, No parity, 9600/19200/38400/57600 /115200bps)	
Simultaneous use of boards	Max. 4	
Software		
OS	Windows 2000/XP/7/8/10 (32/64bit)	
API	Windows Client DLL API	
Development		
Support	Sample Program	VC++
Environmental conditions		
Operating temperature range	0 ~ 60℃	
Storage temperature range	-20 ~ 80℃	
Humidity range	5 ~ 95%	Non-condensing
Board size	120.8mm X 68mm	PCB Board Size

1-2 Product Applications

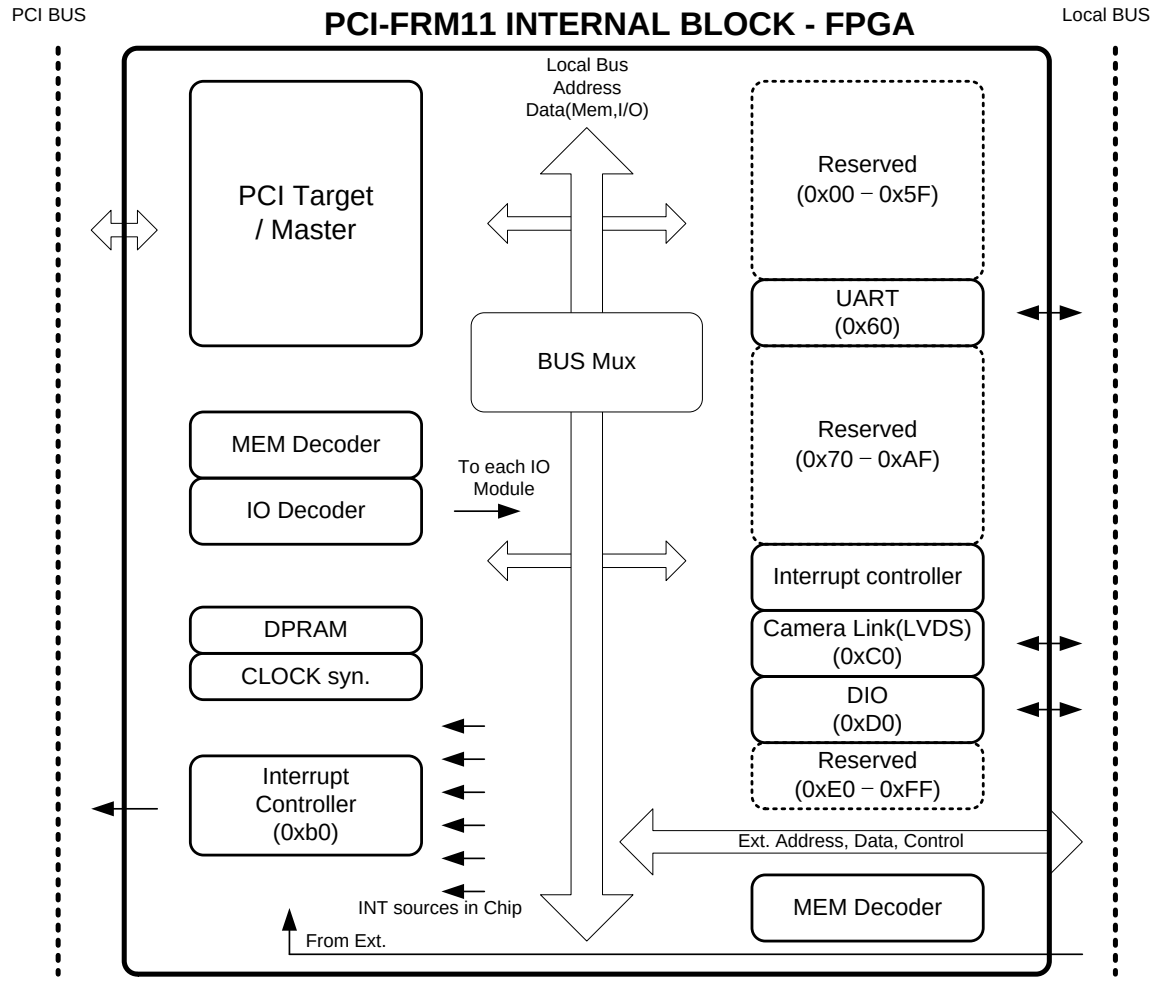
- Image recognition (Pattern, particle, etc.)
- Inspection equipment (Sensor, Semiconductor, Device etc.)
- Black and White, Color Image Display
- Medical Image Capture (X-ray, Supersonic etc.)

2. PCI-FRM11 Board Function

2-1 Board Block Diagram

As shown in the figure below, in the case of PCI-FRM11, FPGA Core Logic is in charge of overall control. Main functions include Frame Data reception, UART data transmission/reception for this, Camera Control signal and external trigger.

These functions are performed using API in PC through PCI interface.



[Figure 2-1. PCI-FRM11 FPGA Block Diagram]

The FPGA core logic is programmed using JTAG, and the logic program is saved in FPGA Program Logic and loaded when power is applied.

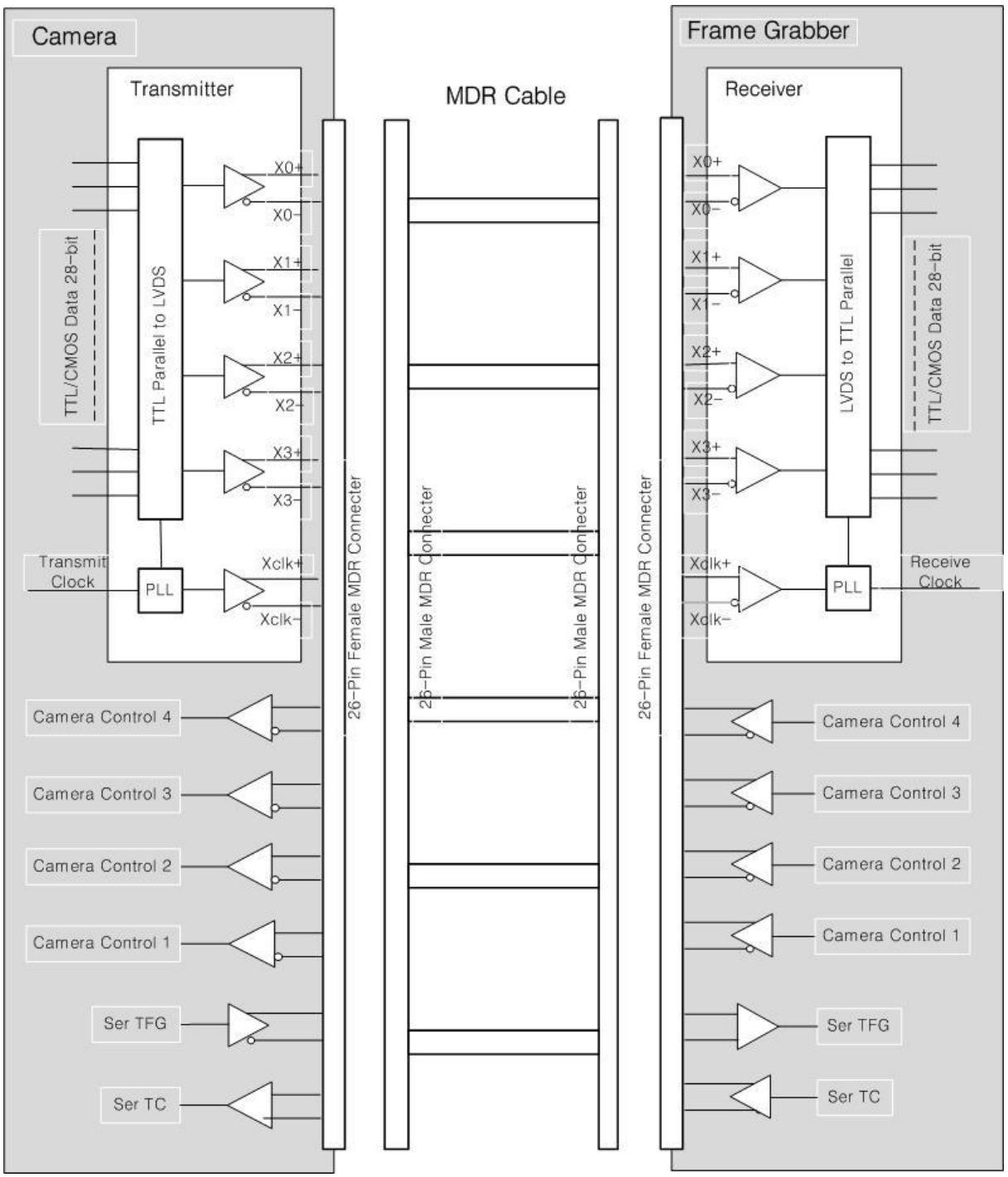
2-2 Camera Link

Camera Link is a communication interface developed for use in vision applications. In the past, we used proprietary connectors and cables between camera makers and frame grabber makers. This caused a lot of confusion and cost increase for users. In order to resolve this confusion, increasing data rate, and confusion in data transmission, the specifications of the Camera Link interface are the specifications of cable or connector assembly, transmission speed and It was made with regulations such as transmission method.

Many digital video solutions today use Low Voltage Differential Signal (LVDS) communication defined by RS-644. RS-644 LVDS has become the Camera Link standard by improving the existing RS-422 method, which had inconvenient cables and limited transmission speed. LVDS can transmit data at high speed by using a differential signal with a low voltage swing. Compared to the existing single-ended signal using one line, the differential signal transmits the signal using two complementary lines. This transmission structure has the characteristics of large-scale common-phase voltage rejection, low power consumption, and excellent noise immunity, which is impossible with single-ended systems that only reference ground for data transmission.

An advanced LVDS technology for the transmission of digital data is a Channel Link. The channel link can transmit parallel-to-serial and serial-to-parallel at 2.38 Gbps. Referring to [Figure 2-3], the transmitter converts 28-bit CMOS/TTL data into 4 LVDS data streams. The converted signal is transmitted to the MDR cable according to the Transmit Clock, and the opposite receiver converts these four LVDS data into a 28-bit CMOS/TTL parallel signal according to the Receive Clock. This channel link technology is being used as a low-cost chipset that is easy to learn and portable, so that it can be used immediately.

Camera Link interface includes Base Configuration, Medium Configuration, and Full Configuration. Base Configuration uses four RS-644 LVDS pairs for transmitter/receiver and camera control as shown in [Figure 2-3], and uses two RS-644 LVDS pairs for communication between camera and frame grabber. The data transmitted serially through the 26-Pin MDR Cable is changed to 28-bit parallel image data at the Receive end of the frame grabber and used.

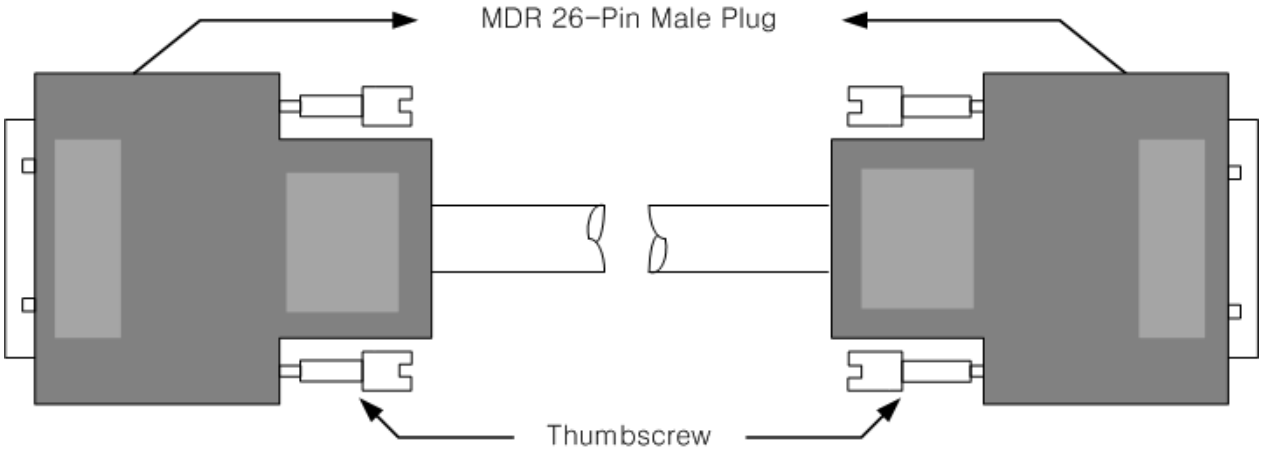


[Figure 2-2. Base Camera Link Block Diagram]

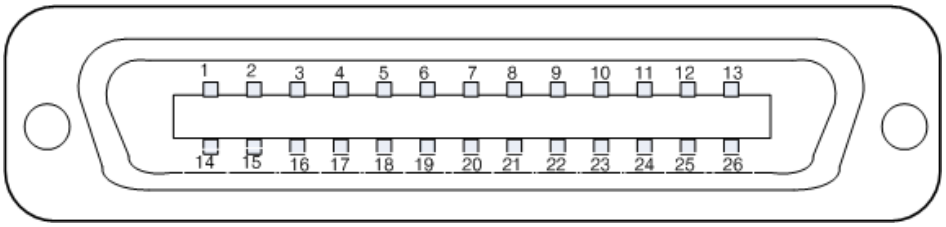
2-3 Camera Link Cable & Connector

Camera Link The connection between the camera and the PCI-FRM11 board uses a 26 Pin MDR (Mini D Ribbon) cable. The camera link cable consists of a twin-axial shielded cable and two MDR 26-male plugs. [Figure 2-3] below is a commonly used camera link cable.

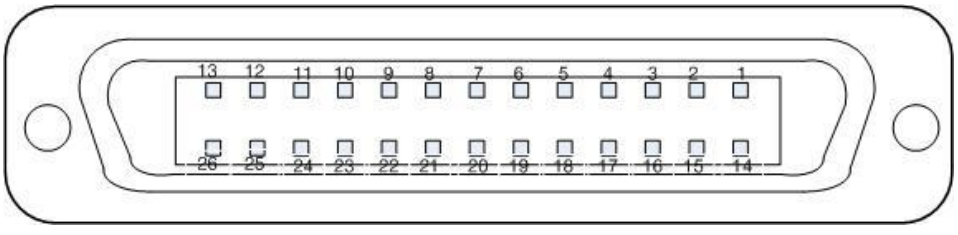
[Figure 2-4] is a 26-Pin Male MDR Connecter located at both ends of the cable, and [Figure 2-5] is a 26-Pin Female MDR Connector, located at the camera or frame grabber. As shown in the figure, the pin numbers are cross-connected, so that the transmitter and receiver terminals of the camera and frame grabber signal lines are cross-connected.



[Figure 2-3. MDR-26 Camera Link Straight Cable]



[Figure 2-4. MDR-26 Cable Pin Map]

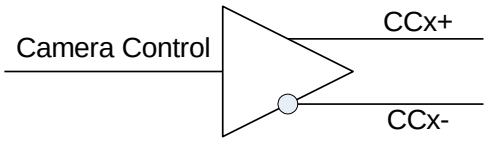


[Figure 2-5. MDR-26 Connector Pin Map(Opposite Connector)]

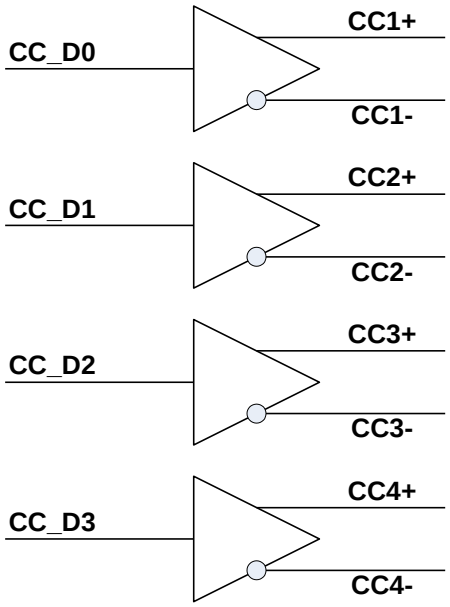
2-4 Camera Link & PCI-FRM11

PCI-FRM11 supports Camera Link Base Configuration. Base Configuration consists of 4 LVDS signal lines serializing 28-bit parallel signals including 24 data bits and 4 enable signals Frame Valid, Line Valid, Data Valid, and a spare, and 1 LVDS signal line to synchronize with the camera. , Asynchronous serial communication including 4 CC (Camera Control) signals and 2 LVDS lines for asynchronous serial communication to communicate with the camera are transmitted through MDR cables.

The transmitted signal deserilizes 4 video LVDS serial signals into 28-bit parallel video signals and control signals (Frame Valid, Line Valid, Data Valid, and a spare) through the Channel Link chip in PCI-FRM11. In addition, a clock signal is made with one LVDS to synchronize the signal between the camera and PCIe-FRM11, and the remaining cameras control signals and communication signals are converted into general TTL signal levels and used.

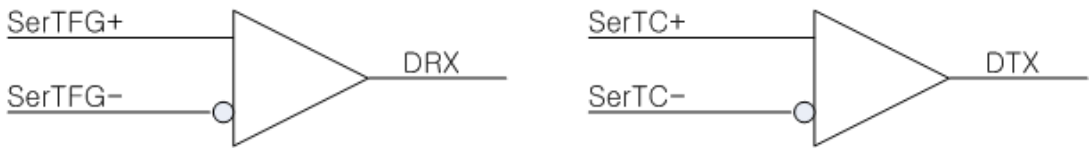


The figure shows the Camera Control output circuit that can send the control signal from the PCI-FRM11 board to the Camera through the Camera-link cable. A total of 4 digital outputs are output through the differential method. Each output is mapped to a digital output and becomes an output. Each bit position is shown in [Figure 2-6] below.



[Figure 2-6. Camera Control LVDS Digital Output Circuit]

The figure below shows the circuit that uses the serial input signal input through the Camera-link cable as a general input on the PCI-FRM11 board.



[Figure 2-7. Serial Communication LVDS Digital Output Circuit]

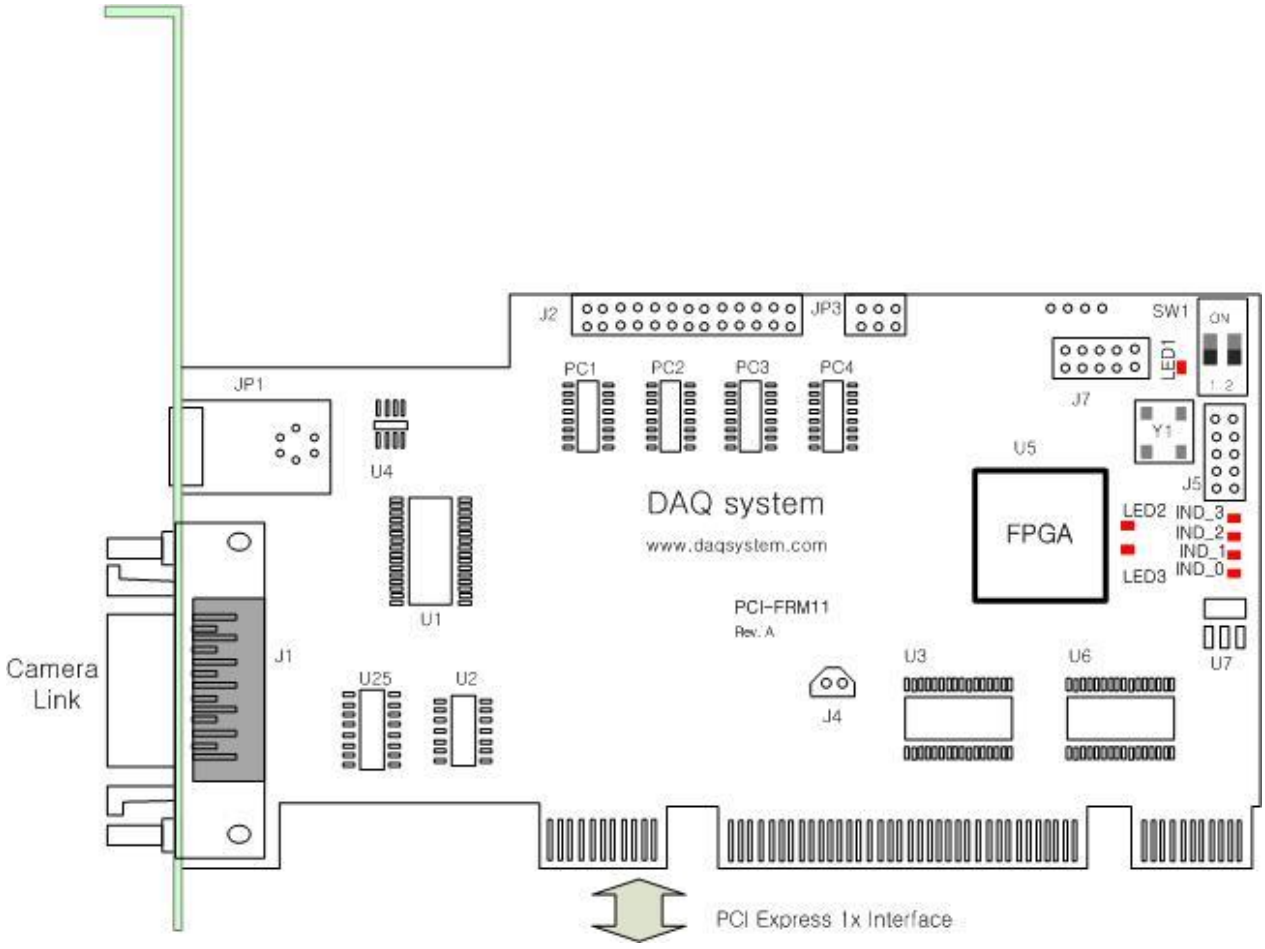
PCI-FRM11 supports Base Configuration including the following bit allocation.

- 1, 2 ,or 3 Pixels (or Taps) at 8 Bits
- 1 or 2 Pixels (or Taps) at 10 Bits
- 1 or 2 Pixels (or Taps) at 12 Bits
- 1 Pixel (or Tap) at 14 Bits
- 1 Pixel (or Tap) at 16 Bits
- 24 Bits RGB

3. PCI-FRM11 Board Description

Each important board function is briefly described. For detailed function information, please refer to the parts specification.

3-1 PCI-FRM11 Board Layout



[Figure 3-1. PCI-FRM11 Layout]

The board has 3 LEDs with indication functions, and the description of each is as follows.

LED2 : Lights up when an image frame is received.

LED3 : Lights up when frame data is being transmitted.

LED1 : Lights up when the board finishes configuration and ready for operation.

3-2 Device Features

(1) **FPGA : U5**

All of the board functions are controlled by the Logic program of the FPGA.

(2) **LVDS : U1**

Receive an image frame.

Transmits/receives UART signals.

Outputs Camera Control Digital Output.

(3) **Regulator : U7**

It supplies the power used by the board.

(4) **Level Shifter : U3, U6**

It protects the circuit by converting the interface of higher voltage than 3.3V CMOS Logic to 3.3V logic level.

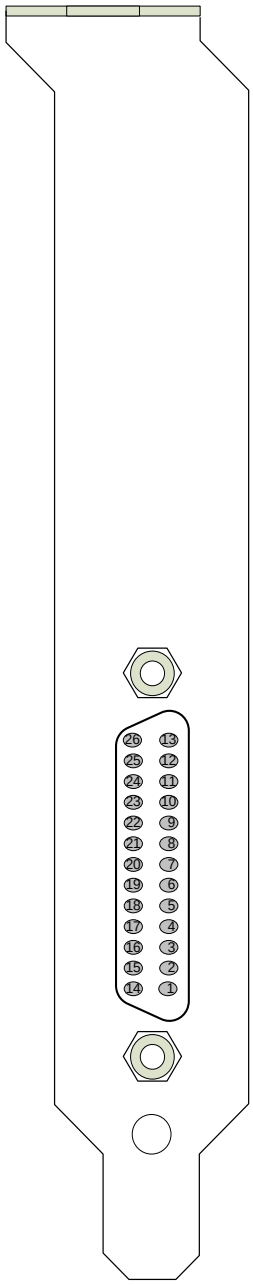
(5) **SW1**

Set the board number.

3-3 Connector Pin-out

This section describes connectors and jumpers used in PCI-FRM11. There is an MDR 26pin connector for the Camera Link connection.

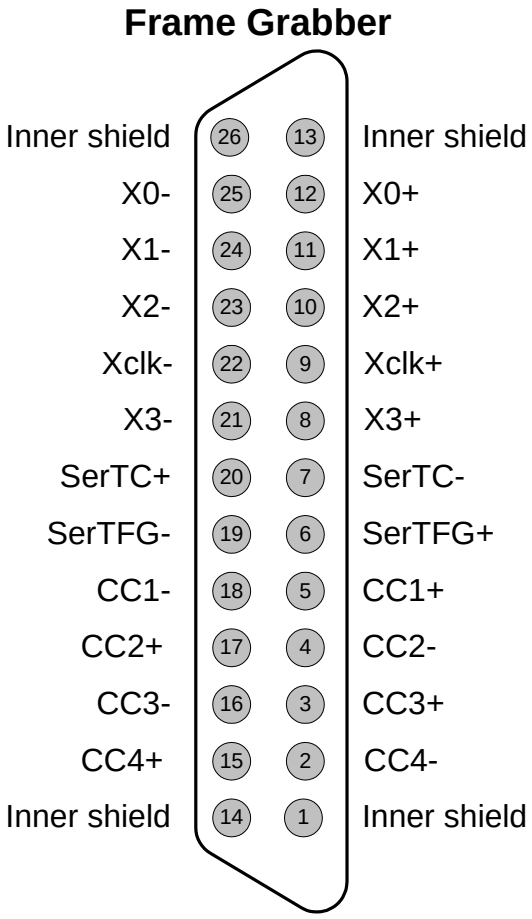
[Figure 3-2] shows the bracket that interfaces with the board and the outside, and the connection connector.



[Figure 3-2. PCI-FRM11 Front View]

3-3-1 J1 (MDR26) Connector

The figure below shows the pin map of the J1 connector of the board used when using the Base Configuration Camera Link. All pin specifications are input/output based on the Camera Link standard, so please refer to the Camera Link standard document for details.



[Figure 3-3. J1 Connector Pin-out]

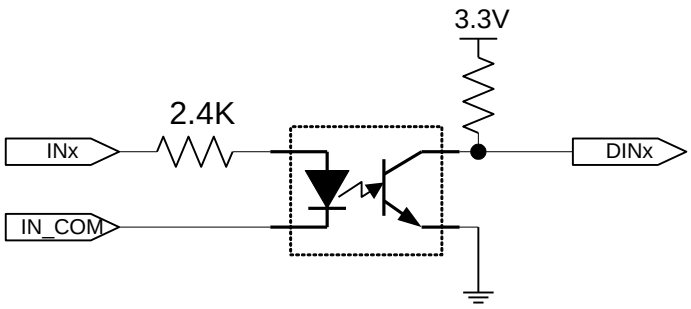
[Table 1. J1 Connector]

Pin No	Name	Description	Remark
1	**Inner Shield**	Cable shield	
2	**CC4-**	Camera Control output 4-	
3	**CC3+**	Camera Control output 3+	
4	**CC2--**	Camera Control output 2-	
5	**CC1+**	Camera Control output 1+	
6	**SerTFG+**	Serial to Frame grabber +	
7	**SerTC-**	Serial to Camera-	
8	**X3+**	Camera link LVDS receive data3 +	
9	**Xclk+**	Camera link LVDS receive clock +	
10	**X2+**	Camera link LVDS receive data2 +	
11	**X1+**	Camera link LVDS receive data1 +	
12	**X0+**	Camera link LVDS receive data0 +	
13	**Inner Shield**		
14	**Inner Shield**		
15	**CC4+**	Camera Control output 4+	
16	**CC3-**	Camera Control output 3-	
17	**CC2+**	Camera Control output 2+	
18	**CC1-**	Camera Control output 1-	
19	**SerTFG-**	Serial to Frame grabber-	
20	**SerTC+**	Serial to Camera+	
21	**X3-**	Camera link LVDS receive data3-	
22	**Xclk-**	Camera link LVDS receive clock-	
23	**X2-**	Camera link LVDS receive data2-	
24	**X1-**	Camera link LVDS receive data1-	
25	**X0-**	Camera link LVDS receive data0-	
26	**Inner Shield**		

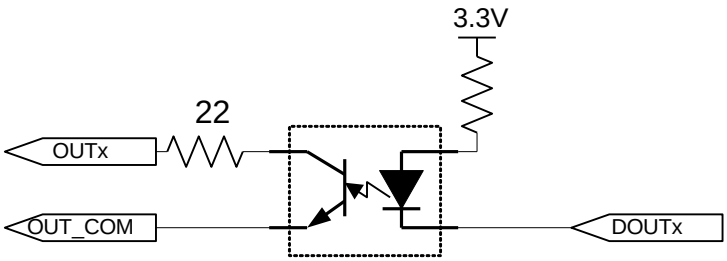
(Note) For more information, refer to Camera Link Standard Specification.

3-3-2 J2 Connector

The PCI-FRM11 board is an external digital input/output device, and 8 digital inputs and 8 digital outputs isolated by a photo-coupler can be used through the J5 connector. The photo-coupler circuit is shown below.



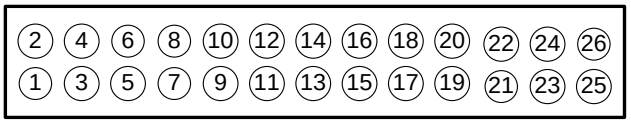
< Photo coupler Input>



<Photo coupler Output>

[Figure 3-4. Photo-coupler Input/Output Circuit]

The pin map of the connector is shown in the figure below.



[Figure 3-5. J2 2x13, 2.53 pitch pin-out]

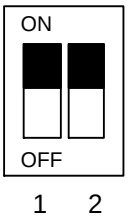
[Table 2. J2 Connector]

Pin No	Name	Description	Remark
1	**DIN0**	Input 0	
2	**DIN4**	Input 4	
3	**DIN1**	Input 1	
4	**DIN5**	Input 5	
5	**DIN2**	Input 2	

6	**DIN6**	Input 6	
7	**DIN3**	Input 3	
8	**DIN7**	Input 7	
9	**DIN_COM**	Input Common	
10	**DIN_COM**	Input Common	
11	**DOUT0**	Output 0	
12	**DOUT4**	Output 4	
13	**DOUT1**	Output 1	
14	**DOUT5**	Output 5	
15	**DOUT2**	Output 2	
16	**DOUT6**	Output 6	
17	**DOUT3**	Output 3	
18	**DOUT7**	Output 7	
19	**DOUT_COM**	Output Common	
20	**DOUT_COM**	Output Common	
21	**N.C**	Not Connect	
22	**N.C**	Not Connect	
23	**GND**	Ground	
24	**GND**	Ground	
25	**+3.3V**	3.3V Power	
26	**+3.3V**	3.3V Power	

3-3-3 SW1 Switch

PCI-FRM11 board is designed to use up to 4 PCIe-FRM11 boards simultaneously in one system (PC). Each board classification can be set through the 4-pin DIP switch in the board.



[Figure 3-6. SW1 Switch (Top View)]

[Table 3. SW1 PIN-OUT]

1	2	Description
OFF	**OFF**	Board No. 0
ON	**OFF**	Board No. 1
OFF	**ON**	Board No. 2
ON	**ON**	Board No. 3

3-3-4 J4 Connector

It is a 3.3V external DC power connector. This is the power used when installing the FPGA and is not normally used.

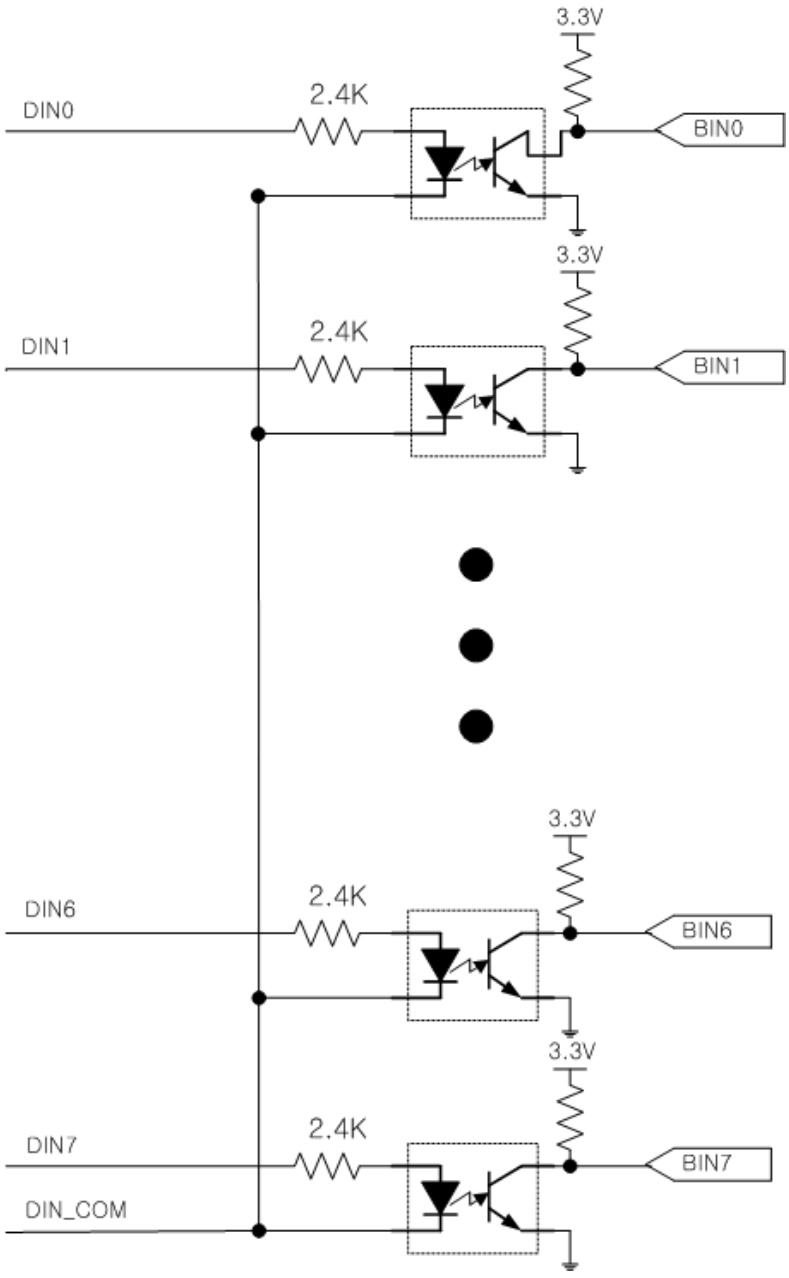
3-3-5 JP3 Connector

JP3 is a JTAG (Joint Test Action Group) connector and is used to update the FPGA program on the board. Do not use when operating the board normally.

3-4 Digital Input/Output

3-4-1 Photo Coupler Input

In the program, input bits 7 to 0 are connected as shown in [Figure 3-7].

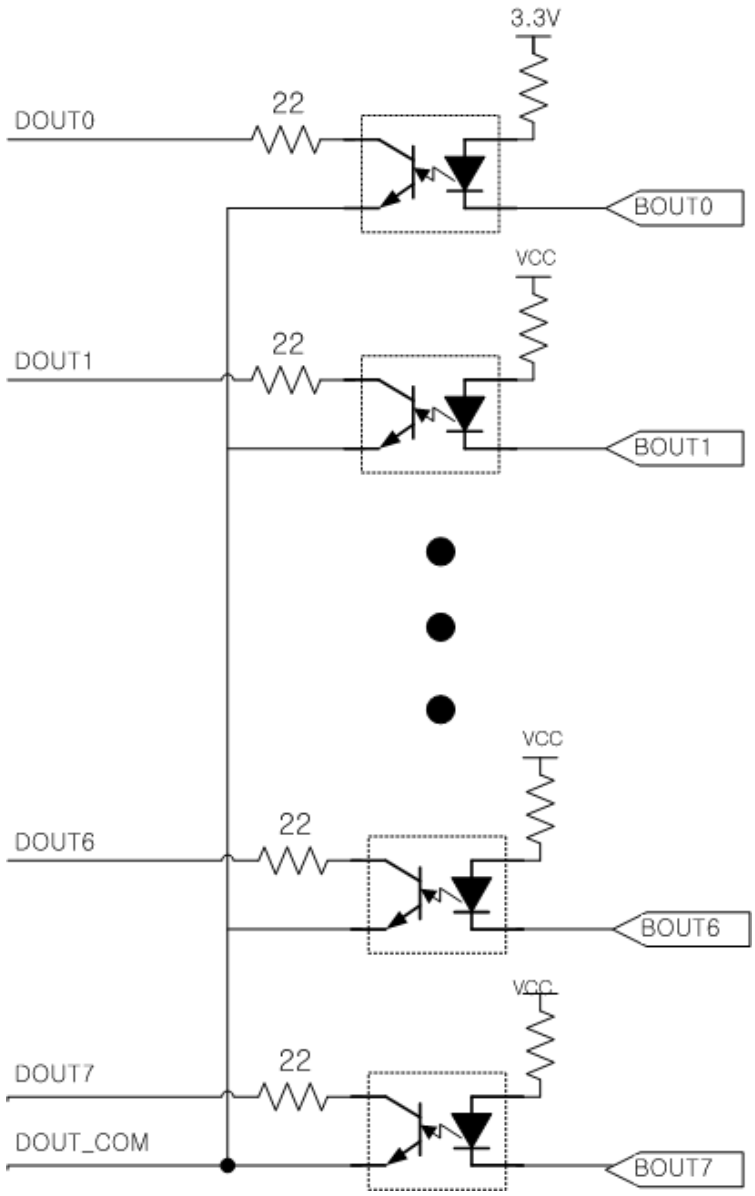


[Figure 3-7. Photo-coupler Digital Input Circuit]

The photo-coupler input can be connected with other DIO boards of the DQ system or connected with a cable (20 pins) through the J2 connector connected to the DSUB 15 pin connector of the PCI-FRM11 board. In this case, only input bits 4 to 0 are connected. .

3-4-2 Photo Coupler Output

In the program, bits 7 to 0 of the output are connected as in [Figure 3-8].



[Figure 3-8. Photo-coupler Digital Output Circuit]

The photo-coupler output can be connected with other DIO boards of the DQ system or connected with a cable (20 pins) through the J2 connector connected to the DSUB 15 pin connector of the PCI-FRM11 board, and in this case, output bits 7 to 0 are connected.

4. Installation

4-1 Product Contents

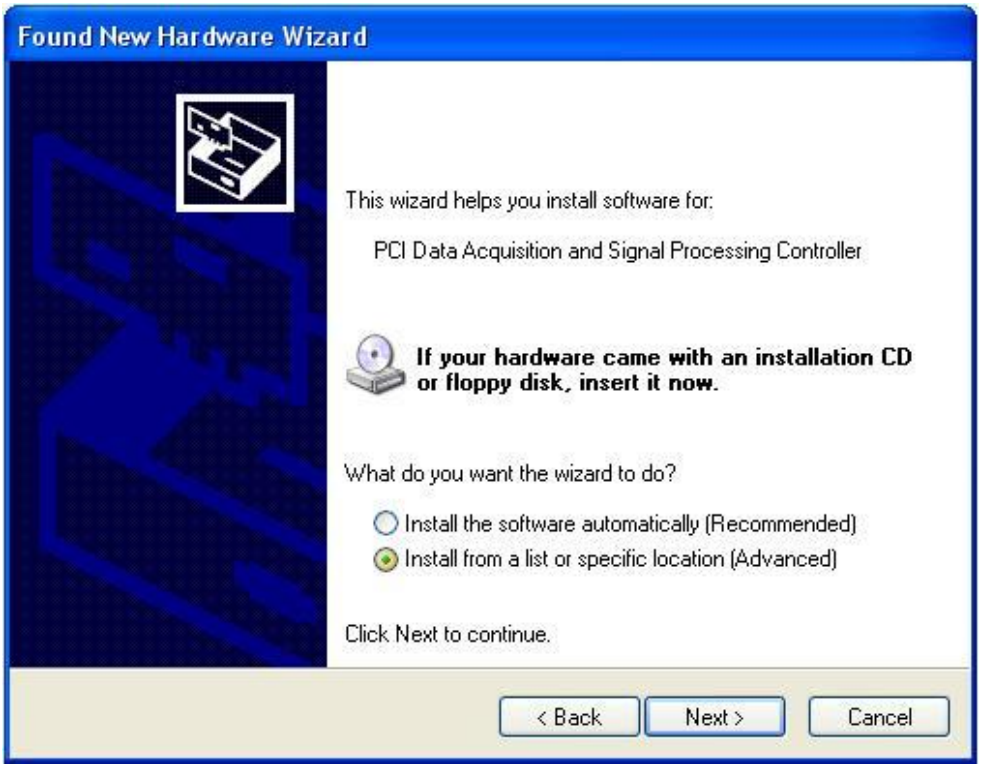
Before installing the board, check that the contents of the package are intact.

1. PCIe-FRM11 Board
2. CD (Drivers/Manual/API/Sample source etc.)

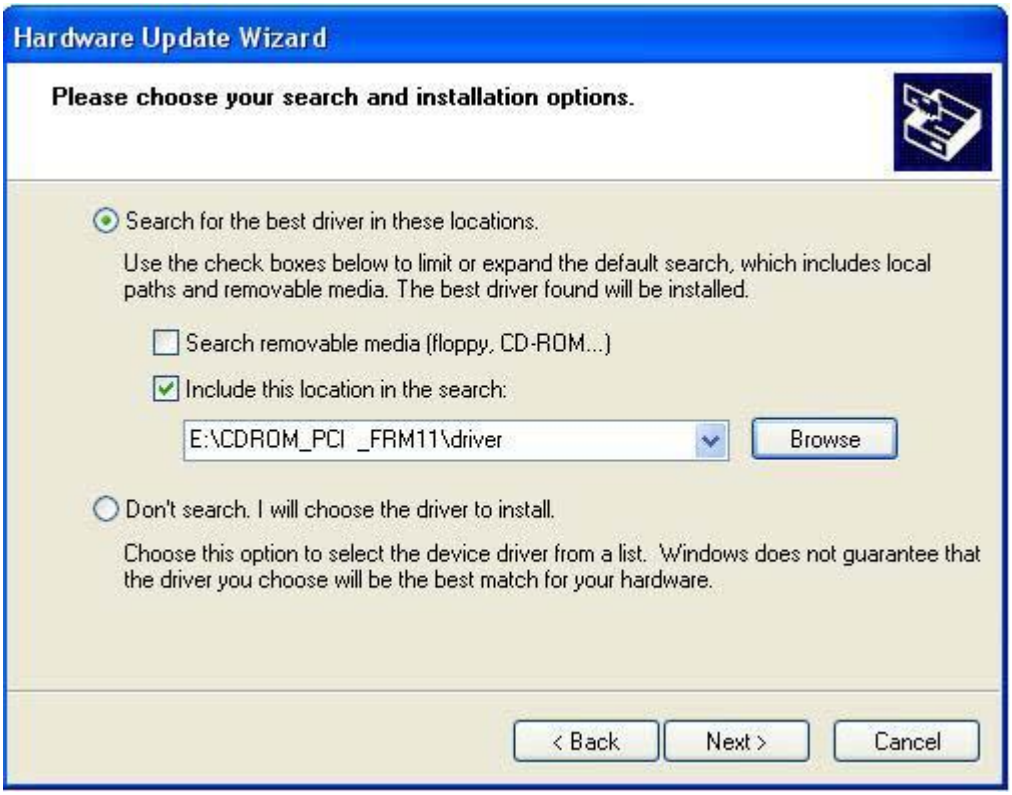
4-2 Installation Process

The board environment must be Windows 2000 SP4 or higher and Windows XP SP1 or higher. First, turn off the PC's power, plug the PCIe-FRM24 board into the PCI Express Slot, and turn on the PC's power. When the "Start New Hardware Wizard" window opens as shown below, select as shown below and click the Next button.

1. Select as below and click the Next button



2. Select Driver from the enclosed CD and click the Next button.



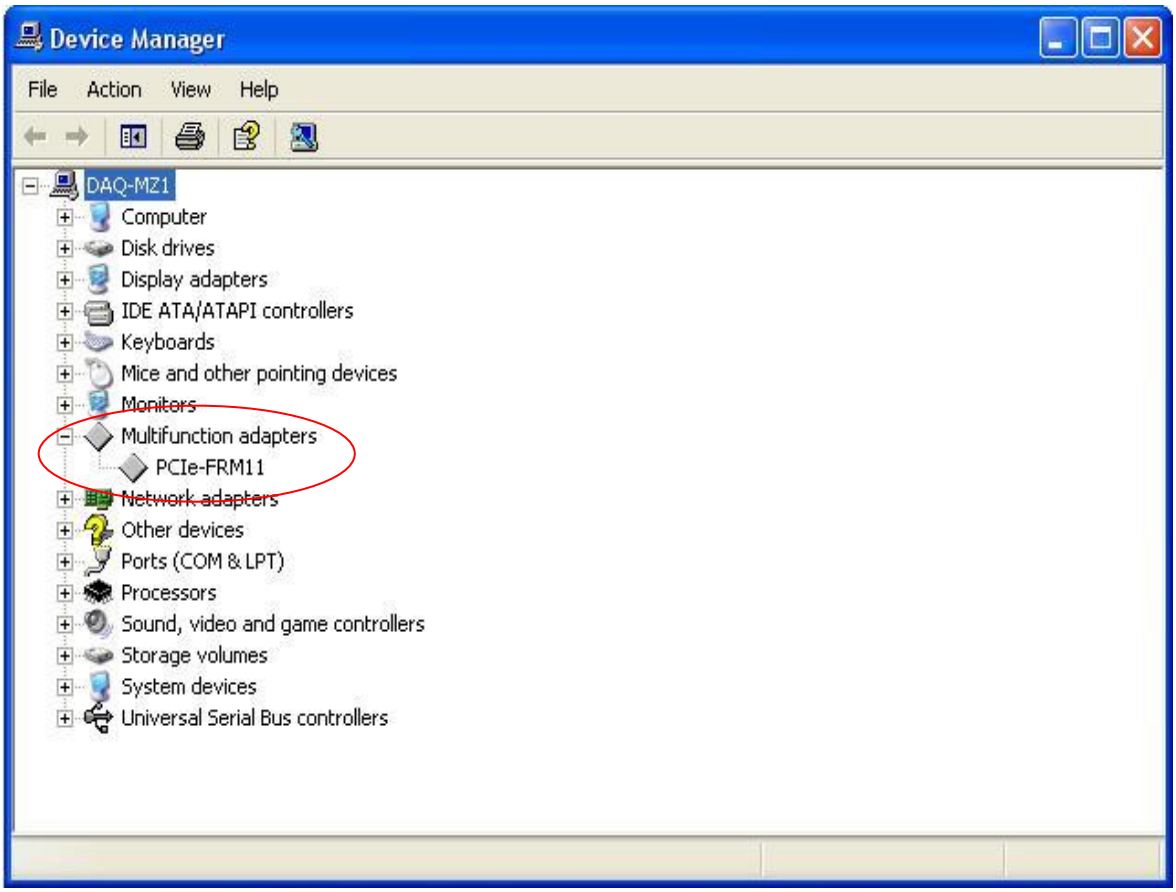
3. Click the Next button. It indicates that the installation process is proceeding as shown below. The driver folder contains **"pcie_frm11.inf"** and **"pcie_frm11.sys"** files required for driver installation. Click Next to install the driver files.

4. When the installation is completed normally, it is shown in the figure below.

5. When the installation is complete, check whether the driver is installed normally in the following way.

6. In My Computer -> Properties -> Hardware -> Device Manager, check if the **Multifunction Adapter -> "PCIe-FRM11"** is installed.

7. If it appears as shown in the figure below, the installation has been completed normally.



If you can see the "PCIe-FRM11" (*The PCI-FRM11 uses a same driver with PCIe-FRM11 because of compatibility.*) at Multifunction Adaptors, the driver installation is to have been over.
(Check the red circle)

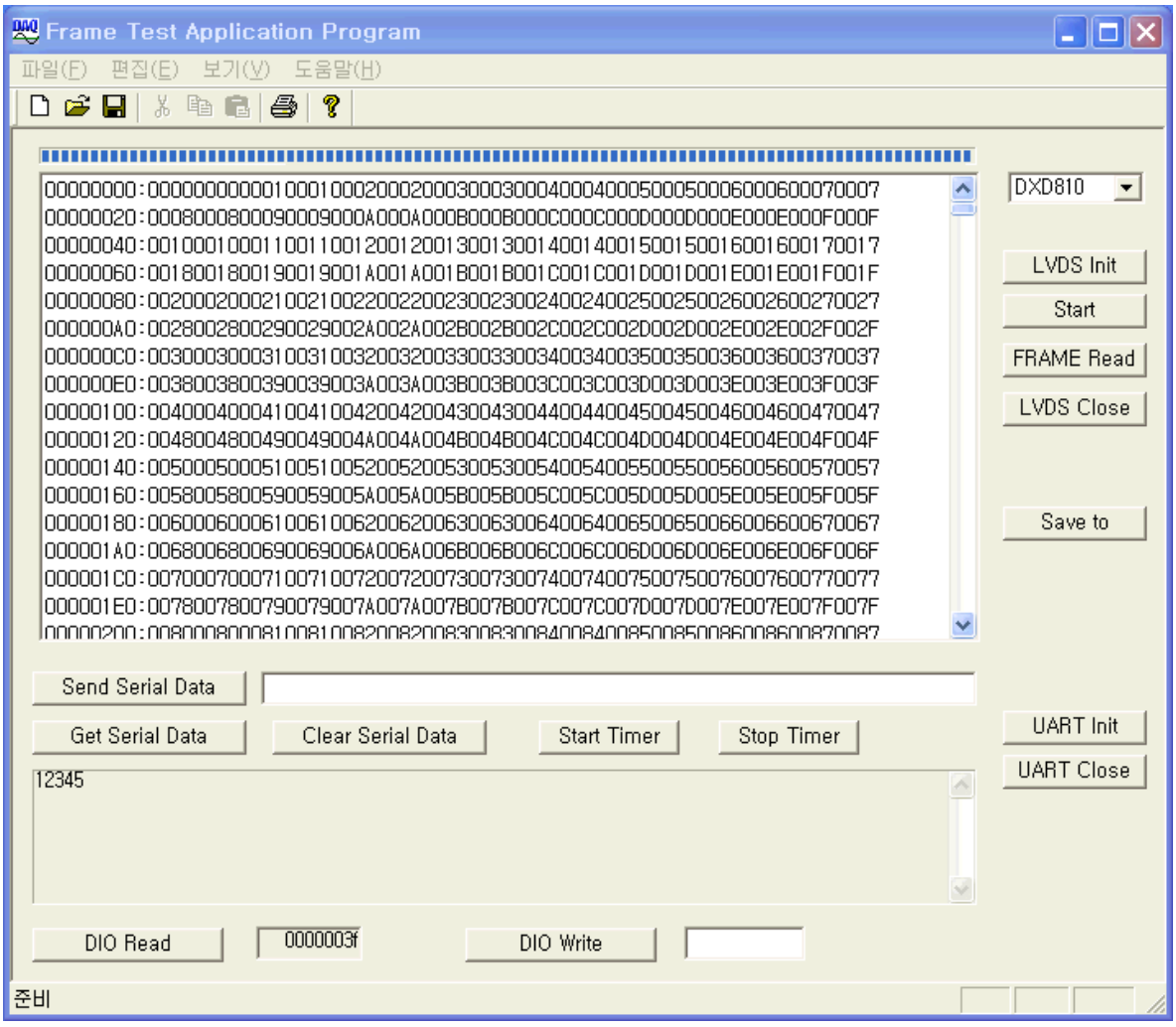
(Note) After initial installation, the PC must be rebooted for normal operation.

5. Sample Program

In the folder of the CDROM provided with the board, "FrmTest" and "FrameView" are provided for easy use of the board. First, "FrmTest.exe", one of the executable files, displays Frame Data as a hexadecimal value and stores it in memory or hard disk so that developers can utilize the frame data needed for it, and "FrameView.exe" It is an executable file that shows the screen as an image for easy understanding of the data by the user. In order to test the sample program, the driver of the board must be installed first.

In order to test the sample program, the driver of the board must be installed first. The sample program is provided in source form so that the API provided to use the board can be tested briefly, so the user can modify it and use it.

5-1 FrmTest Program



[Figure 5-1. Sample Program "FrmTest.exe"]

API (Application Programming Interface) is required to use the above sample program. API is provided in the form of "DLL", and import library and header file are required to compile. All files specified above are included on the supplied CDROM. In order to run the sample program normally, the API DLL **(pci_frm11.dll)** must be in the folder of the executable file or in the Windows system folder or the folder specified by the Path environment variable

5-1-1 Image Frame Function

(1) '**DXD810/DXD1417'** Combo-box

Use this box to set up the operation mode.

(2) '**LVDS Init'** button

Press this button to initialize the function of receiving image frame data. It is performed only once after power is applied to the board.

(3) '**Start'** button

Press this button to begin to save image data from Camera Link.

(4) '**FRAME Read'** button

Press this button to read the image frame data of the board to your PC. If image frame data is not saved on the board, you must wait until the end of data collection.

(5) '**LVDS Close'** button

Press this button to finish usage of the board and terminate the program.

(6) '**Save to'** button

Press this button to save the image frame data.

5-1-2 UART Function

(1) '**Send Serial Data'** button

Press this button to send the data in the editor box to UART. You can directly write the data in the editor box beside the button.

(2) '**Get Serial Data'** button

Press this button to get the data on the general UART.

(3) '**Clear Serial Data'** button

Press this button to clear the contents of the editor box.

(4) '**Start Timer'** button

Press this button to start the timer. The sample program will read the UART data periodically. The reading interval is around 0.1s.

(5) '**Stop Timer'** button

Press this button to stop the timer.

(6) '**UART Init'** button

Press this button to initialize UART. It must be performed only once after power is applied to the board.

(7) '**UART Close'** button

Press this button to finish usage of the board and terminate the program.

5-1-3 DIO Function

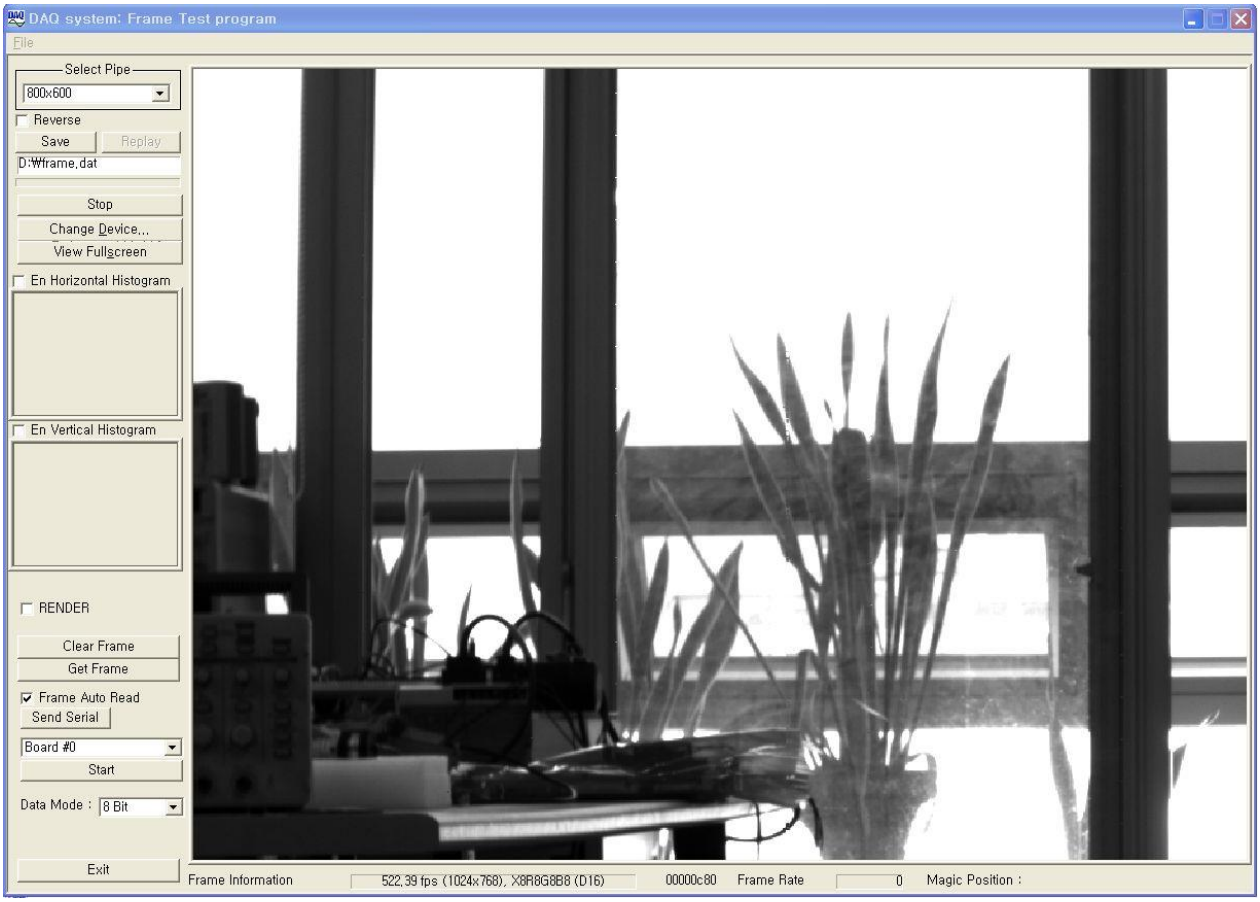
(1) '**DIO Read'** button

Press this button to read the data on General Purpose I/O port. It will be written an editor box.

(2) '**DIO Write'** button

Press this button to write the data on General Purpose I/O port. You can directly write the data in the editor box beside the button.

5-2 FrameView Program



[Figure 5-2. Sample Program "FrameView.exe"]

API (Application Programming Interface) is required to use the above sample program. API is provided in the form of "DLL", and import library and header file are required to compile.

All files specified above are included on the supplied CDROM. In order to run the sample program normally, the API DLL (PCI_FRM11.DLL) must be located in the folder of the executable file or in the Windows system folder or the folder specified by the Path environment variable.

[Figure 5-2] is a screen captured by connecting a Camera-Link camera to PCI-FRM11 and executing "FrameView.exe" on the image displayed on the monitor. The description of each menu bar is as follows.

(1) Select Pipe

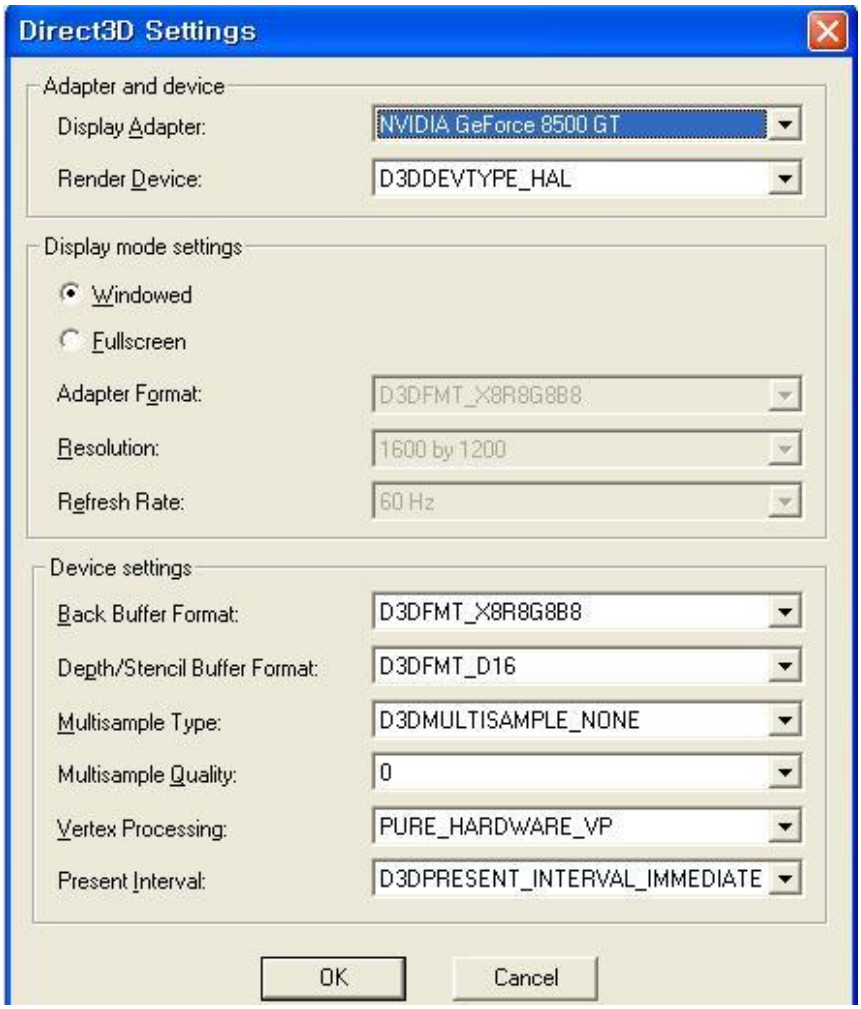
Display resolution – Select it as fitted to input resolution.

Reverse --- Reverse On/Off

(2) Save --- Save to D:₩frame.dat. (It is fixed.)

(3) Stop --- Stop the saving.

(4) Change Device --- Select a device which you wanted, if several devices are stick.



(5) View Fullscreen --- A screen shows all over an image.

(6) Render --- If you check, display a video. Otherwise, display a still frame.

(7) Board Number --- Select a PCI-FRM11 board number (0 ~ 3)

(8) Start --- Start a program.

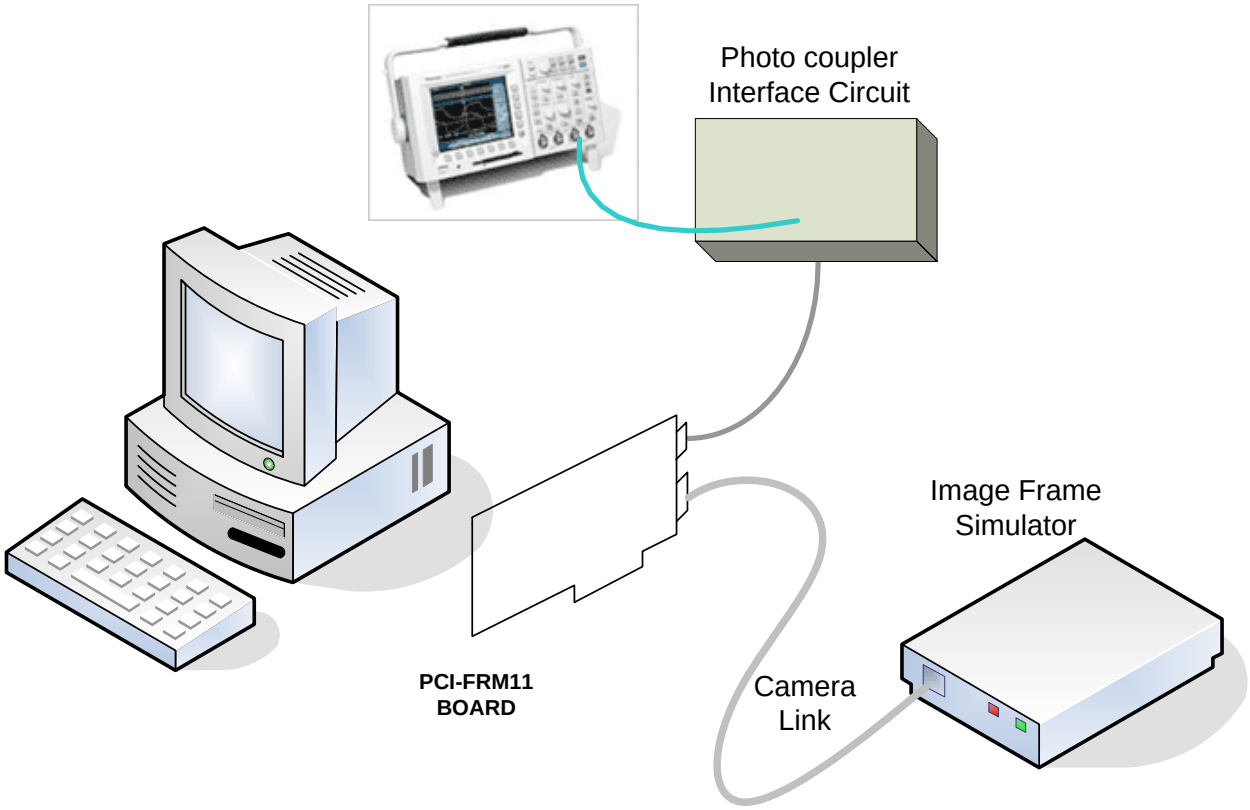
(9) Data Mode --- 8, 16, 24 bit selection

(10) Exit --- Exit a program.

6. Test

6-1 Image Frame Test

In this chapter, we will conduct a functional test to learn whether there is any abnormality in the board and how to use it briefly. The test is executed using the sample program ("FrmTest.exe") in the PC where the PCI-FRM11 board is installed.



[Figure 6-1. Equipment Connection for Testing]

In the picture above, the PCI-FRM11 board is installed in the PC, but the picture is drawn outside for better understanding. The image frame simulator is self-made by the DAQ system, and if you have an actual device, you can use it.

Complete the wiring as shown in the figure above and apply power. After confirming that the PCI-FRM11 board is registered in the PC, run the sample program ("FrmTest.exe") on the PC.

(1) After initializing by pressing the "LVDS init" button, click the "Start" button to save the image frame.

(2) Press the "Frame Read" button to load the image data of the program. The read data is displayed in the editor box, so check whether it matches the actual data sent. In some cases, it is necessary to use a separate verification program, so press the "Save to" button to save the read data as a file and check whether there is any abnormality in the data.

6-2 UART Tx/Rx Test

In the above connection state, the image frame simulator periodically transmits serial data to the board.

(1) After initialization by pressing the UART init button, press the "Start Timer" button to periodically read the UART data transmitted from the simulator and display it on the screen.

(2) As shown in [Figure 5-1], write the text to be transmitted in the editor box next to the "Send Serial Data" button and press the button to transmit the UART data. The transmitted data is checked in the simulator.

6-3 DIO Test

Continue the test in the above connection condition.

(1) Make sure that all output ports are "1" with "DIO Write" function and check with the oscilloscope. In order to check the LVDS output and the photo-coupler output with an oscilloscope, an external circuit configuration is required.

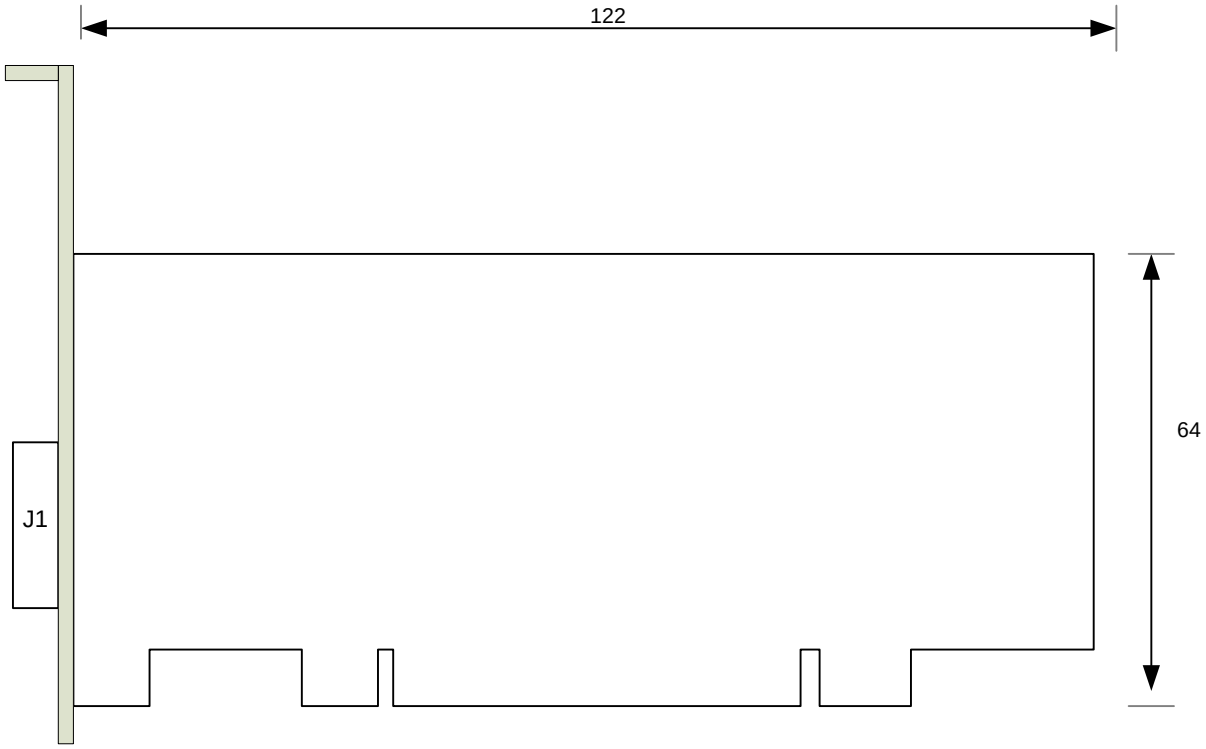
(2) Check the input with "DIO Read" function. At this time, test the photo-coupler and a separate external circuit for LVDS input.

Appendix

A-1 Board Size

The external sizes of the board are as follows.

For detailed dimensions, please contact the person in charge.



A-2 Repair Regulations

Thank you for purchasing a DAQ SYSTEM product. Please refer to the following regarding Customer Service regulated by DAQ SYSTEM.

(1) Read the user manual and follow the instructions before using the DAQ SYSTEM product.

(2) When returning the product to be repaired, please write down the symptoms of the failure and send it to the head office.

(3) All DAQ SYSTEM products have a 1-year warranty.
- -. Warranty period counts from the date the product is shipped from DAQ SYSTEM.
- -. Peripherals and third-party products not manufactured by DAQ SYSTEM are covered by the manufacturer's warranty.
- -. If you need repairs, please contact the Contact Point below..

(4) Even during the warranty period, repairs are charged in the following cases..
- ① Failure or damage caused by use without following the user's manual
- ② Failure or damage caused by customer's negligence during product transportation after purchase
- ③ Failure or damage caused by natural phenomena such as fire, earthquake, flood, lightning, pollution, or power supply exceeding the recommended range
- ④ Failure or damage caused by inappropriate storage environment (e.g. high temperature, high humidity, volatile chemicals, etc.)
- ⑤ Breakdown or damage due to unreasonable repair or modification
- ⑥ Products whose serial number has been changed or removed intentionally
- ⑦ If DAQ SYSTEM determines that it is the customer's fault for other reasons

(5) Shipping costs for returning the repaired product to DAQ SYSTEM are the responsibility of the customer.

(6) The manufacturer is not responsible for any problems caused by misuse, regardless of our warranty terms.

References

1. Specification of Camera Link Interface Standard for Digital Cameras and Frame Grabbers
-- Camera Link committee
2. PCI Local Bus Specification Revision2.1
-- PCI Special Interest Group
3. AN201 How to build application using API
-- DAQ system
4. AN312 PCI-FRM11 API Programming
-- DAQ system

MEMO

Contact Point

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