PCI-DSP01

Reference Manual

Contents

PCI-DSP01 Memory MAP

1. TMS320C6205 Memory map

Table 1. TMS320C6201/C6205/C6701 DSP Memory Map

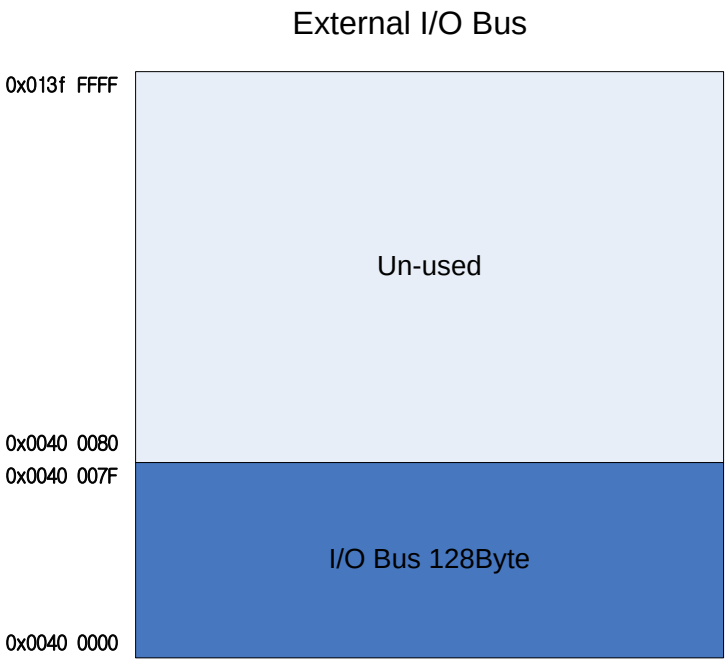
Address Range (Hex)	Size (Bytes)	MAP 0	MAP 1
0000 0000–0000 FFFF	64K	External memory interface CE0	Internal program RAM
0001 0000–003F FFFF	4M–64K	External memory interface CE0	Reserved
0040 0000–00FF FFFF	12M	External memory interface CE0	External memory interface CE0
0100 0000–013F FFFF	4M	External memory interface CE1	External memory interface CE0
0140 0000–0140 FFFF	64K	Internal program RAM	External memory interface CE1
0141 0000–017F FFFF	4M–64K	Reserved	External memory interface CE1
0180 0000–0183 FFFF	256K	Internal peripheral bus EMIF registers	
0184 0000–0187 FFFF	256K	Internal peripheral bus DMA controller registers	
0188 0000–018B FFFF	256K	Internal peripheral bus HPI registers (C6201/C6701 DSP)†	
018C 0000–018F FFFF	256K	Internal peripheral bus McBSP0 registers	
0190 0000–0193 FFFF	256K	Internal peripheral bus McBSP1 registers	
0194 0000–0197 FFFF	256K	Internal peripheral bus timer0 registers	
0198 0000–019B FFFF	256K	Internal peripheral bus timer1 registers	
019C 0000–019F FFFF	256K	Internal peripheral bus interrupt selector registers	
01A0 0000–01A3 FFFF	256K	Reserved	
01A4 0000–01A8 FFFF	320K	Internal peripheral bus PCI registers (C6205 DSP only)†	
01A9 0000–01FF FFFF	6M–576K	Internal peripheral bus (reserved)	
0200 0000–02FF FFFF	16M	External memory interface CE2	
0300 0000–03FF FFFF	16M	External memory interface CE3	
0400 0000–3FFF FFFF	1G–64M	Reserved	
4000 0000–4FFF FFFF	256M	Reserved	
5000 0000–5FFF FFFF	256M	Reserved	
6000 0000–6FFF FFFF	256M	Reserved	
7000 0000–7FFF FFFF	256M	Reserved	
8000 0000–8000 FFFF	64K	Internal data RAM	
8001 0000–FFFF FFFF	2G–64K	Reserved	

† Address range is reserved on other devices.

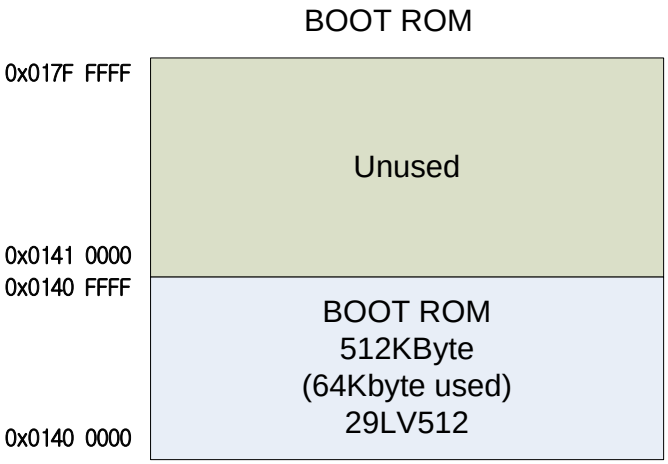
<Map summary >

(Note 1) Default memory map is MAP1(Factory setting)

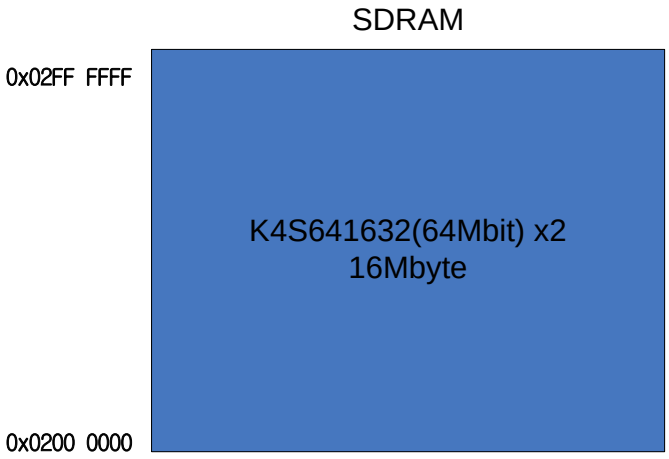
2. EMIF CE0 (I/O Bus)



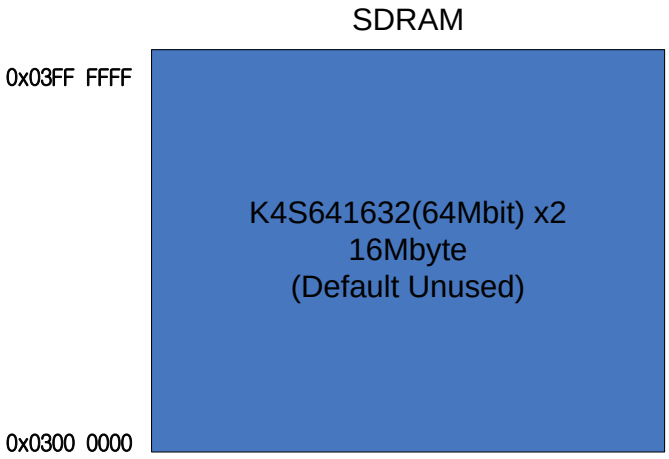
3. EMIF CE1 (BOOT ROM)



4. EMIF CE2 (SDRAM, 16Mbyte)



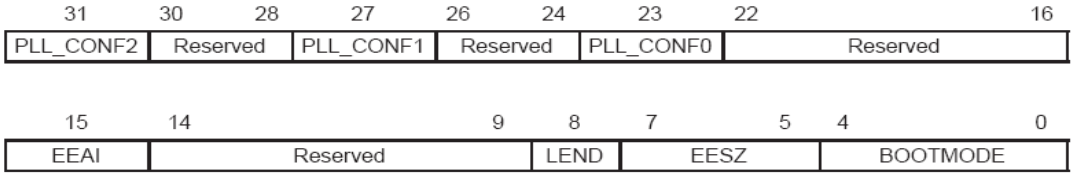
5. EMIF CE3 (SDRAM, 16Mbyte)



6. TMS320C6205-BOOT MODE

BOOTMODE[4:0]	Memory Map	Memory at Address 0	Boot Process
00000	MAP 0	SDRAM: SDWID = 0 (512 elements per row)†	None
00001	MAP 0	SDRAM: SDWID = 1 (256 elements per row)†	None
00010	MAP 0	32-bit asynchronous with default timing	None
00011	MAP 0	1/2× rate SBSRAM	None
00100	MAP 0	1× rate SBSRAM	None
00101	MAP 1	Internal	None
00110	MAP 0	External: default values	Host boot (HPI/XBUS/PCI)
00111	MAP 1	Internal	Host boot (HPI/XBUS/PCI)
01000	MAP 0	SDRAM: four 8-bit devices (SDWID = 0)	8-bit ROM with default timings
01001	MAP 0	SDRAM: two16-bit devices (SDWID = 1)	8-bit ROM with default timings
01010	MAP 0	32-bit asynchronous with default timing	8-bit ROM with default timings
01011	MAP 0	1/2× rate SBSRAM	8-bit ROM with default timings
01100	MAP 0	1× rate SBSRAM	8-bit ROM with default timings
01101	MAP 1	Internal	8-bit ROM with default timings
01110–01111	–	Reserved	–
10000	MAP 0	SDRAM: four 8-bit devices(SDWID=0)	16-bit ROM with default timings
10001	MAP 0	SDRAM: two 16-bit devices (SDWID = 1)	16-bit ROM with default timings
10010	MAP 0	32-bit asynchronous with default timing	16-bit ROM with default timings
10011	MAP 0	1/2× rate SBSRAM	16-bit ROM with default timings
10100	MAP 0	1× rate SBSRAM	16-bit ROM with default timings
10101	MAP 1	Internal	16-bit ROM with default timings
10110–10111	–	Reserved	–
11000	MAP 0	SDRAM: four 8-bit devices (SDWID = 0)	32-bit ROM with default timings
11001	MAP 0	SDRAM: two 16-bit devices (SDWID = 1)	32-bit ROM with default timings
11010	MAP 0	32-bit asynchronous with default timing	32-bit ROM with default timings
11011	MAP 0	1/2× rate SBSRAM	32-bit ROM with default timings
11100	MAP 0	1× rate SBSRAM	32-bit ROM with default timings
11101	MAP 1	Internal	32-bit ROM with default timings
11110–11111	–	Reserved	–

Figure 2. TMS320C6205 DSP Boot and Device Configuration via Pull-Up/Pull-Down Resistors on ED[31:0]



† All reserved fields should be pulled down.

Table 7. TMS320C6205 DSP Boot and Device Configuration Description

ED Bit	Field	Value	Description
31	PLL_CONF2		On-chip PLL is enabled or disabled by CLKMODE0 pin. When CLKMODE0 = 0, on-chip PLL is bypassed. When CLKMODE0 = 1, CPU clock is determined by PLL_CONF2, PLL_CONF1, and PLL_CONF0 bits. See Table 8. Note that CLKMODE0 acts as a PLL enable pin and the ED pins (pins 31, 27, and 23) determine the PLL multiplier option.
30–28	Reserved	0	Reserved. The reserved field should be pulled down.
27	PLL_CONF1		On-chip PLL is enabled or disabled by CLKMODE0 pin. When CLKMODE0 = 0, on-chip PLL is bypassed. When CLKMODE0 = 1, CPU clock is determined by PLL_CONF2, PLL_CONF1, and PLL_CONF0 bits. See Table 8. Note that CLKMODE0 acts as a PLL enable pin and the ED pins (pins 31, 27, and 23) determine the PLL multiplier option.
26–24	Reserved	0	Reserved. The reserved field should be pulled down.
23	PLL_CONF0		On-chip PLL is enabled or disabled by CLKMODE0 pin. When CLKMODE0 = 0, on-chip PLL is bypassed. When CLKMODE0 = 1, CPU clock is determined by PLL_CONF2, PLL_CONF1, and PLL_CONF0 bits. See Table 8. Note that CLKMODE0 acts as a PLL enable pin and the ED pins (pins 31, 27, and 23) determine the PLL multiplier option.
22–16	Reserved	0	Reserved. The reserved field should be pulled down.
15	EEAI		EEPROM autoinitialization.
		0	PCI uses default values.
		1	Read configure value from EEPROM.
14–9	Reserved	0	Reserved. The reserved field should be pulled down.
8	LEND		Little endian mode.
		0	System operates in big-endian mode.
		1	System operates in little-endian mode.
7–5	EESZ	0–7h	EEPROM size selection (EEPROM is always 16-bit).
		0	No EEPROM
		1h	1K
		2h	2K
		3h	4K
		4h	16K
		5h–7h	Reserved
4–0	BOOTMODE	0–1Fh	Determines the boot-mode of the device. See Table 5.

Table 8. CPU Clock Rate as Determined by PLL_CONFn Bits (C6205 DSP)

PLL_CONF*n* Bits (ED[31, 27, 23])	CPU Clock Rate
000	CLKIN × 1 (PLL Bypass)
001	CLKIN × 4
010	CLKIN × 8
011	CLKIN × 10
100	CLKIN × 6
101	CLKIN × 9
110	CLKIN × 7
111	CLKIN × 11

7. EEPROM contents

Table 5. EEPROM Memory Map

Address	Contents (msb ... lsb)
0h	Vendor ID
1h	Device ID
2h	Class Code [7–0]/Revision ID
3h	Class Code [23–8]
4h	Subsystem Vendor ID
5h	Subsystem ID
6h	Max_Latency/Min_Grant
7h	PC_D1/PC_D0 (power consumed D1, D0)
8h	PC_D3/PC_D2 (power consumed D3, D2)
9h	PD_D1/PD_D0 (power dissipated D1, D0)
Ah	PD_D3/PD_D2 (power dissipated D3, D2)
Bh	Data_scale (PD_D3....PC_D0)
Ch	0000 0000 PMC[14–9], PMC[5], PMC[3]
Dh	Checksum

EEPROM Checksum

The configuration data contained in the EEPROM is checked against a checksum. The checksum is a 16-bit cumulative exclusive-OR (XOR) of the configuration data words contained in the EEPROM starting with an initial value of AAAAh. You must ensure that the proper 16-bit checksum value is written to address 0Dh when programming the EEPROM.

Checksum = AAAAh XOR Data(00h) XOR Data(01h)….. XOR Data(0Dh)

If the checksum fails, the CFGERR bit in PCIIS and in HSR are set, and optionally, an interrupt to the DSP is generated. The DSP may or may not catch the interrupt, depending on the state of the core at the time. If the PCI is booting the device, the core is held in reset and will miss the interrupt.

The EEREAD bit in HSR is set, if EEPROM autoinitialization is used at power-on reset.

If the serial EEPROM is not accessed for PCI configuration purposes (that is, EEAI = 0, EESZ = 000b at reset), then the checksum is not performed.

Failed checksums result in the PCI configuration registers being initialized with default data. Refer to the specific PCI configuration registers to determine their default values (see section 16.1).

After successful PCI configuration register initialization (auto or default), the CFGDONE bit in RSTSRC is updated to allow the DSP to respond to reads, rather than terminating the cycle with disconnect retry.

8. PCI Configuration Registers

Table 7. PCI Configuration Registers

Address	Access	Byte 3	Byte 2	Byte 1	Byte 0
00h	read only	Device ID		Vendor ID	
04h	read/write	Status		Command	
08h	read only	Class Code			Revision ID
0Ch	read/write	Reserved	Header Type	Latency Timer	Cache Line Size
10h	read/write	Base 0 Address (4M-byte prefetchable)			
14h	read/write	Base 1 Address (8M-byte nonprefetchable)			
18h	read/write	Base 2 Address (4 words I/O)			
24h	read only	Reserved			
2Ch	read only	Subsystem ID		Subsystem Vendor ID	
30h	read only	Reserved			
34h	read only	Reserved			Capabilities Pointer
38h	read only	Reserved			
3Ch	read/write	Max_Latency	Min_Grant	Interrupt Pin	Interrupt Line
40h	read only	Power Management Capabilities		Next Item Pointer	Capability ID
44h	read/write	Power Data	Reserved	Power Management Control/Status	
48h FFh	read only	Reserved			

Note: Shaded registers can be autoloaded from EEPROM at autoinitialization.

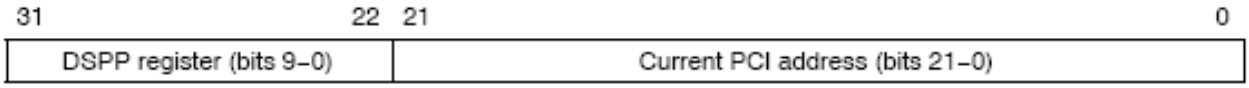
9. PCI Memory Map

The PCI port has full visibility into the DSP memory map through three base address registers:

- Base 0: 4M-byte prefetchable maps to all of DSP memory with the DSP page register (DSPP). Prefetch reads have all bytes valid.
- Base 1: 8M-byte nonprefetchable maps to DSP memory-mapped registers. Nonprefetch supports byte enables.
- Base 2: 16-byte I/O contains I/O registers for the PCI host

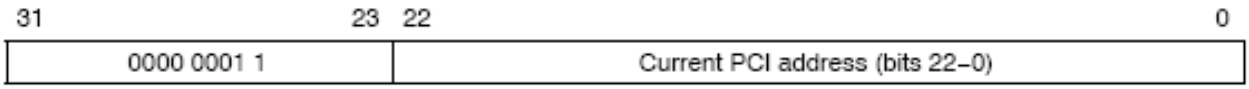
The DSPP, described in section 16.2.3, is used to locate the 4M-byte window within the DSP memory map. Bits 21–0 of the PCI address are concatenated with bits 9–0 of DSPP to form the DSP address for PCI slave access to the DSP as shown in Figure 4.

Figure 4. PCI Base Slave Address Generation (Prefetchable)



The PCI base 1 register on the DSP is configured for an 8M-byte nonprefetchable region. This memory is mapped into the DSP at a fixed location (0180000h–0200000h). Bits 22–0 of the PCI address are concatenated with a fixed offset to map the base 1 access into the memory-mapped registers as shown in Figure 5.

Figure 5. PCI Base 1 Slave Address Generation (Nonprefetchable)



Base address register 2 is configured for a 16-byte I/O region for the PCI host to access the PCI I/O registers. See section 16.2.

Table 36. PCI Memory-Mapped Registers

Acronym	Register Name	Section
RSTSRC	DSP reset source/status register	16.3.1
PMDCSR†	Power management DSP control/status register	16.3.2
PCIIS	PCI interrupt source register	16.3.3
PCIIEN	PCI interrupt enable register	16.3.4
DSPMA	DSP master address register	16.3.5
PCIMA	PCI master address register	16.3.6
PCIMC	PCI master control register	16.3.7
CDSPA	Current DSP address register	16.3.8
CPCIA	Current PCI address register	16.3.9
CCNT	Current byte count register	16.3.10
EEADD	EEPROM address register	16.3.11
EEDAT	EEPROM data register	16.3.12
EECTL	EEPROM control register	16.3.13
HALT†	PCI transfer halt register	16.3.14
TRCTL‡	PCI transfer request control register	16.3.15

† This register only applies to C62x/C67x DSP.
‡ TRCTL register only applies to C64x DSP.

10. PCI I/O Map

PCI I/O Registers Accessed via I/O Space (Base 2 Memory)

Address†	Register/Port Accessed
I/O Base Address + 00h	Host status register (HSR)
I/O Base Address + 04h	Host-to-DSP control register (HDCR)
I/O Base Address + 08h	DSP page register (DSPP)
I/O Base Address + 0Ch	Reserved

16.2.1 Host Status Register (HSR)

The host status register (HSR) is shown in Figure 30 and described in Table 33.

Figure 30. Host Status Register (HSR)

31	8
Reserved†	
HR-0	

7	5	4	3	2	1	0
Reserved†		EEREAD	CFGERR	INTAM	INTAVAL	INTSRC
HR-0		HR-x	HR-0	HR/W-1	HR-0	HR/W-0

Legend: H = Host access; R = Read only; R/W = Read/Write; -*n* = value after reset; -x = value is indeterminate after reset
† If writing to this field, always write the default value for future device compatibility.

Table 33. Host Status Register (HSR) Field Descriptions

Bit	Field	Value	Description
31–5	Reserved	0	Reserved. The reserved bit location always returns the default value. A value written to this field has no effect. If writing to this field, always write the default value for future device compatibility.
4	EEREAD		Indicates if the PCI configuration registers were initialized from EEPROM. Host read-only bit, writes have no effect. Reset source is $\overline{\text{PRST}}$.
		0	PCI configuration registers were initialized from default values.
		1	PCI configuration registers were initialized from EEPROM.
3	CFGERR		Indicates if an autoinitialization configuration error occurred. Host read-only bit, writes have no effect. Reset source is $\overline{\text{PRST}}$.
		0	No error occurred.
		1	Autoinitialization configuration error occurred.
2	INTAM		$\overline{\text{PINTA}}$ mask. Disables DSP assertion of $\overline{\text{PINTA}}$. Only written by the PCI host (during D1, D2, or D3, the $\overline{\text{PINTA}}$ is masked by the power management logic). Reset source is $\overline{\text{PRST}}$.
		0	$\overline{\text{PINTA}}$ is asserted by the DSP when the INTREQ bit in the DSP reset source/status register (RSTSRC) is set.
		1	$\overline{\text{PINTA}}$ is not asserted. Note that this does not reset the interrupt generating logic, you must set the INTRST bit in the DSP reset source/status register (RSTSRC).

1	INTAVAL		Indicates the current $\overline{\text{PINTA}}$ pin value. Host read-only bit, writes have no effect. $\overline{\text{PINTA}}$ can be deasserted by the PCI host writing a 1 to the INTSRC bit or by the DSP writing a 1 to the INTRST bit in the DSP reset source/status register (RSTSRC). Reset source is $\overline{\text{PRST}}$.
		0	$\overline{\text{PINTA}}$ is not asserted (inactive).
		1	$\overline{\text{PINTA}}$ is asserted (active).
0	INTSRC		PCI IRQ source active since last HSR clear. This bit, when 1, indicates that the DSP asserted the $\overline{\text{PINTA}}$ interrupt by writing the INTREQ bit in the DSP reset source/status register (RSTSRC), and the INTAM bit was 0. Reset source is $\overline{\text{PRST}}$. This bit can be cleared by the PCI host by writing a 1 to this bit. This also negates the $\overline{\text{PINTA}}$ signal.
		0	For reads, $\overline{\text{PINTA}}$ was not asserted after last clear. For writes, no affect.
		1	For reads, $\overline{\text{PINTA}}$ was asserted after last clear. For writes, deassert $\overline{\text{PINTA}}$. Note that this does not enable future interrupts. The INTRST bit in RSTSRC must also be set to allow future interrupts. See section 16.3.1.

16.2.2 Host-to-DSP Control Register (HDCR)

The host-to-DSP control register (HDCR) is shown in Figure 31 and described in Table 34.

Figure 31. Host-to-DSP Control Register (HDCR)

31	8
Reserved†	
HR-0	

7	3	2	1	0
Reserved†		PCIBOOT	DSPINT	WARMRESET
HR-0		HR-0	HW-0	HW-0

Legend: H = Host access; R = Read only; W = Write only; -*n* = value after reset
† If writing to this field, always write the default value for future device compatibility.

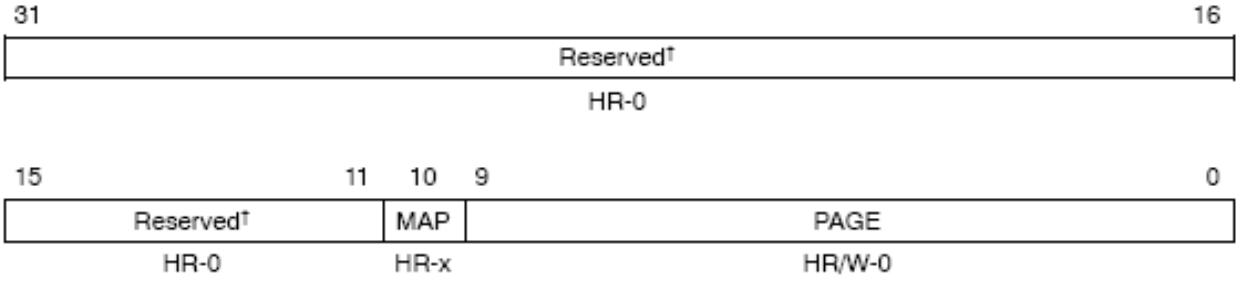
Table 34. Host-to-DSP Control Register (HDCR) Field Descriptions

Bit	Field	Value	Description
31–3	Reserved	0	Reserved. The reserved bit location always returns the default value. A value written to this field has no effect. If writing to this field, always write the default value for future device compatibility.
2	PCIBOOT		PCI boot mode. Host read-only bit, writes have no effect. Reset source is $\overline{\text{RESET}}$.
		0	DSP does not boot from the PCI.
		1	DSP boots from the PCI.
1	DSPINT		DSP interrupt. Host write-only bit, reads return 0.
			The interrupt is generated to the core via the HOSTSW bit in the PCI interrupt source register (PCIIS). If booting from the PCI interface, this interrupt takes the core out of reset. In all other cases, the DSP core must have its clock running and the HOSTSW bit in the PCI interrupt enable register (PCIIEN) unmasked in order to latch the interrupt. Reset source is $\overline{\text{PRST}}$.
		0	A write of 0 is ignored.
		1	Generates a host interrupt to the DSP.
0	WARMRESET		DSP warm reset. Host write-only bit.
			WARMRESET only applies in D0. WARMRESET should not be used if the core is in power management state D1, D2, or D3 (I/O access is disabled in these states). Reset source is $\overline{\text{RESET}}$.
		0	A write of 0 is ignored.
		1	Resets the DSP. The DSP is held in reset for 16 PCI cycles. The DSP cannot be accessed until 16 PCI clocks after WARMRESET is written.

16.2.3 DSP Page Register (DSPP)

The DSP page register (DSPP) is shown in Figure 32 and described in Table 35.

Figure 32. DSP Page Register (DSPP)



Legend: H = Host access; R = Read only; R/W = Read/Write; -*n* = value after reset; -x = value is indeterminate after reset
† If writing to this field, always write the default value for future device compatibility.

Table 35. DSP Page Register (DSPP) Field Descriptions

Bit	Field	Value	Description
31–11	Reserved	0	Reserved. The reserved bit location always returns the default value. A value written to this field has no effect. If writing to this field, always write the default value for future device compatibility.
10	MAP		Indicates the memory map being used by the DSP (C62x/C67x DSP only). Host read-only bit, writes have no effect. Reset source is RESET.
		0	Map 0
		1	Map 1
9–0	PAGE	0–3FFh	Locates a 4M-byte memory window within the DSP address map for prefetchable (base 0) memory accesses. Reset source is PRST.

11. External Memory Interface Registers

Table 2–10. EMIF Registers for C620x/C670x DSP

Acronym	Register Name	Hex Byte Address	Section
GBLCTL	EMIF global control register	0180 0000h	2.8.1
CECTL0	EMIF CE0 space control register	0180 0008h	2.8.2
CECTL1	EMIF CE1 space control register	0180 0004h	2.8.2
CECTL2	EMIF CE2 space control register	0180 0010h	2.8.2
CECTL3	EMIF CE3 space control register	0180 0014h	2.8.2
SDCTL	EMIF SDRAM control register	0180 0018h	2.8.3
SDTIM	EMIF SDRAM refresh control register	0180 001Ch	2.8.4

12. McBSP Registers

Table 17. McBSP Registers for C620x/C670x DSP

		McBSPs on Device (Hex Byte Address)			
Acronym	Register Name	McBSP 0	McBSP 1	McBSP 2§	Section
RBR†	Receive buffer register	–	–	–	–
RSR†	Receive shift register	–	–	–	–
XSR†	Transmit shift register	–	–	–	–
DRR‡	Data receive register	018C 0000	0190 0000	01A4 0000	11.1
DXR	Data transmit register	018C 0004	0190 0004	01A4 0004	11.2
SPCR	Serial port control register	018C 0008	0190 0008	01A4 0008	11.3
RCR	Receive control register	018C 000C	0190 000C	01A4 000C	11.4
XCR	Transmit control register	018C 0010	0190 0010	01A4 0010	11.5
SRGR	Sample rate generator register	018C 0014	0190 0014	01A4 0014	11.6
MCR	Multichannel control register	018C 0018	0190 0018	01A4 0018	11.7
RCER	Receive channel enable register	018C 001C	0190 001C	01A4 001C	11.8
XCER	Transmit channel enable register	018C 0020	0190 0020	01A4 0020	11.9
PCR	Pin control register	018C 0024	0190 0024	01A4 0024	11.12

† The RBR, RSR, and XSR are not directly accessible via the CPU or the DMA/EDMA controller.
‡ The CPU and DMA/EDMA controller can only read this register; they cannot write to it.
§ Available only on C6202(B) DSP and C6203(B) DSP.

13. PCI Memory-Mapped Registers

Table 36. PCI Memory-Mapped Registers

Acronym	Register Name	Section
RSTSRC	DSP reset source/status register	16.3.1
PMDCSR†	Power management DSP control/status register	16.3.2
PCIIS	PCI interrupt source register	16.3.3
PCIIEN	PCI interrupt enable register	16.3.4
DSPMA	DSP master address register	16.3.5
PCIMA	PCI master address register	16.3.6
PCIMC	PCI master control register	16.3.7
CDSPA	Current DSP address register	16.3.8
CPCIA	Current PCI address register	16.3.9
CCNT	Current byte count register	16.3.10
EEADD	EEPROM address register	16.3.11
EEDAT	EEPROM data register	16.3.12
EECTL	EEPROM control register	16.3.13
HALT†	PCI transfer halt register	16.3.14
TRCTL‡	PCI transfer request control register	16.3.15

† This register only applies to C62x/C67x DSP.
‡ TRCTL register only applies to C64x DSP.

